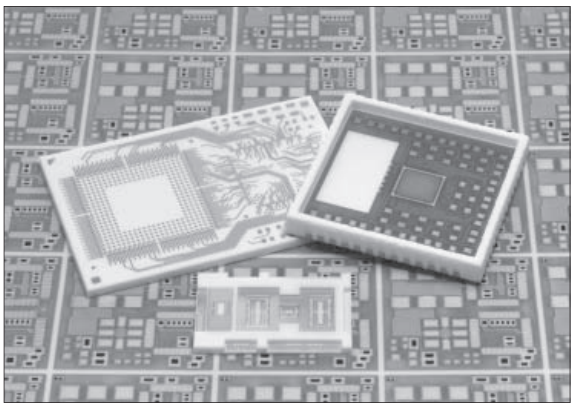
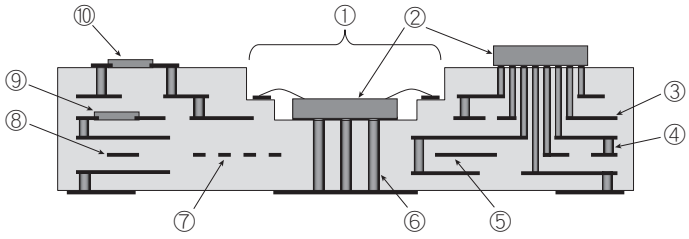
LOW TEMPERATURE CO-FIRED CERAMICS

EU RoHS

KLC LTCC低温共烧陶瓷多层基板
LTCC Multilayer Substrates



■ 结构图　Construction



①	空腔	Cavity	⑥	散热孔	Thermal via
②	IC芯片	IC-chip	⑦	电感器	Inductor
③	导线分布图	Conductor pattern	⑧	传送线路	Transmission line
④	通过	Via	⑨	内层电阻	Buried resistor
⑤	电容器	Capacitor	⑩	表层电阻	Surface resistor

■ LTCC是什么　What is LTCC?

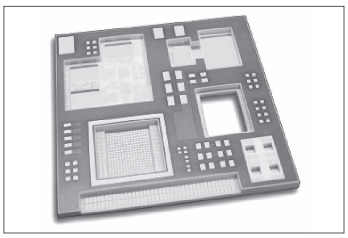
LTCC是Low Temperature Co-fired Ceramics（低温同步煅烧陶瓷）的缩写。通过在氧化铝中加玻璃系材质，能比传统的陶瓷电路板以“低温”煅烧，是可与低电阻导体同时煅烧的陶瓷多层电路板。
KOA LTCC将导体电阻小的Ag导体材料作为配线图案，在陶瓷内以多层构造而一体成型（同时煅烧）。
由此，可以制成因导体电阻成分而造成的损失很少的电气特性优异、尺寸精度高的多层电路板。此外，由于电阻体和传输线路在表层和内层能以多层构造而一体成型，因此有利于小型化。再加上热膨胀系数与硅胶近似，因此有利于裸芯片的贴装，通过在空腔内贴装，可实现电路板的低背化。
LTCC, which stands for Low Temperature Co-fired Ceramics, is multilayer Ceramic substrate. This substrate makes it possible to use low resistive conductor as conductor patterns in it by the lower temperature firing process than general ceramic firing process by adding glass to alumina.
KOA's LTCC can be used Ag as conductor patterns, and formed multilayer structure with the co-firing process.
Therefore, low loss electric performance and high dimensional accuracy are achieved.
KOA's LTCC is advantage for downsizing by forming surface resistors, inner resistors, and embedding transmission lines on/in the substrate. In addition, thermal expansion coefficient that is close to silicon's enhances the reliability of the bare chip mounting, and mounting chip in a cavity makes possible low profile packages.

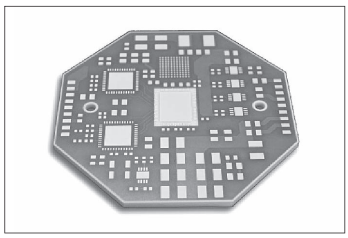
■ 特点　Features

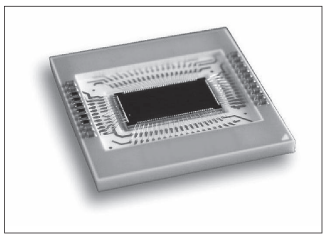
- 由于热膨胀系数接近硅胶，且具有优异的尺寸精度和平坦性，很适合封装裸芯片。
- 由于采用感应损失低的陶瓷以及损失很小的导体，因此具有优异的高频率特性。
- 通过多层配线、多腔构造、形成向内层与表层的小型印刷电阻，可实现小型、高集成化。
- 可进行圆形、多角形、凹凸状等特殊外形及空腔形状的成型。
- 裸芯片贴装部设有散热孔，可进一步提高散热性。
- 由于是陶瓷，因此耐热性、耐湿性优异，不会产生气体或尘埃。
- 符合欧盟RoHS。
- The substrates are suitable for the bare chip mounting, as the thermal expansion coefficient is close to silicon's, and dimension accuracy and flatness are excellent.
- By the uses of low dielectric-loss ceramics and low loss conductors, the substrates excel in the high frequency characteristics.
- Miniaturization and high integration are possible by the multilayer wiring, the multi-cavity structure and the surface / buried printing resistors.
- The special shapes of substrate and cavity such as circle shape, polygonal shape and concavo-convex shape are available.
- Thermal vias under bare chips can improve thermal conductivity of the substrate.
- The substrates are outstanding in heat resistance and humidity resistance and non-occurrence of outgas due to the ceramics used.

■ 用途　Applications

- 使用微波、毫米波等的高频率的用途。
- 在高温、高湿度等环境严酷的环境下也可以使用。
- 各种传感器封装。
- 裸形片多芯片模块。
- MEMS包装。
- 转接基板
- Applications using high frequencies like micro-waves, milli-waves, etc.
- Applications used in harsh environment, especially in high temperatures, high humidities, etc.
- Various sensor packages.
- Multi chip modules for bare chips.
- MEMS packages.
- Interposer substrates.







■ 品名构成　Type Designation

实例　Example

KLC	AB1
品种 Product Code	制造密码 KOA Ref. No.

欲知关于此产品含有的环境负荷物质详情（除EU-RoHS以外），请与我们联系。
Contact us when you have control request for environmental hazardous material other than the substance specified by EU-RoHS.

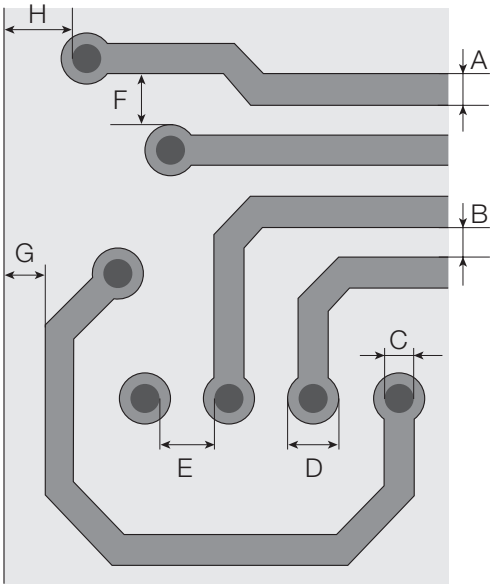
■ 基板材料特性　Characteristics of Substrate Material

项目 Parameter	特性 Characteristics
抗析强度（MPa） Bending strength	250
热膨胀系数（×10^{-6}/K） Thermal expansion coefficient	5.5
热传导率（W/m • K） Thermal conductivity	3
绝缘电阻（Ω • cm） Insulation resistance	＞10^{13}
介电常数 at 1MHz Dielectric constant	7
介质损耗 at 1MHz Dielectric loss	＜0.003
内部导体电阻（μΩ • cm） Resistivity of buried conductor	Ag 2.5
密度（g/cm^3） Density	2.8
表面光洁度 Ra（μm） Surface roughness Ra	＜0.4
耐压（kV/mm） Withstanding voltage	＞15
层厚（μm/Layer） Layer thickness	80, 100, 125 STD.

■ 设计规则　Design rule

符号 Symbol	项目 Parameter	设计值 Design value
A	线路宽度 Line width	0.06mm Min.
B	线路间空间 Line to line spacing	0.06mm Min.
C	通路直径 Via diameter	0.1mm, 0.15mm, 0.2mm
D	通路充填直径 Via pad diameter	Via diameter＋0.05mm Min.
E	通路间隔 Via to via spacing	0.2mm Min.
F	通路－线路间隔 Via to line spacing	0.15mm Min.
G	模型层通路充填直径 Part edge to conductor spacing	0.2mm Min.
H	基板端模型间隔 Part edge to Via spacing	0.3mm Min.
J1，J2	空腔宽度 Cavity width	0.6mm Min.
K1，K2	空腔深度 Cavity depth	0.1mm Min.
L	空腔壁面厚度 Wall thickness of cavity	0.5mm Min.
M	空腔内隔板宽度 Shelf width in the cavity	0.5mm Min.

表层 • 内层　Surface layer ・Inner layer



空腔　Cavity