iC-MQF PROGRAMMABLE 12-BIT Sin/Cos INTERPOLATION IC WITH RS422 DRIVER

preliminary

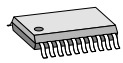
FEATURES

- Latency-free sine-to-digital conversion to 4000 angle steps
- Input frequency: 200 kHz (x10), 20 kHz (x100), 2 kHz (x1000)
- Flexible pin assignment due to signal path multiplexers
- PGA inputs for differential and single-ended signals
- Variable input resistance for current/voltage conversion
- Signal conditioning for offset, amplitude and phase
- Controlled 50 mA current source for LED or MR sensor supply
- Fault-tolerant RS422 outputs with 50 mA sink/source drive current
- Preselectable minimum phase distance for spike-proof counter stimulus
- Zero signal conditioning and electronic index pulse generation
- Signal and operation monitoring with configurable alarm output, output shutdown and error storage
- I^2C multimaster interface for in-circuit calibration and parameters (EEPROM)
- Adjustable overtemperature alarm and shutdown
- Supply from 4.3 to 5.5 V, operation from -40 to +100 °C
- Reverse-polarity-proof including the sub-system

APPLICATIONS

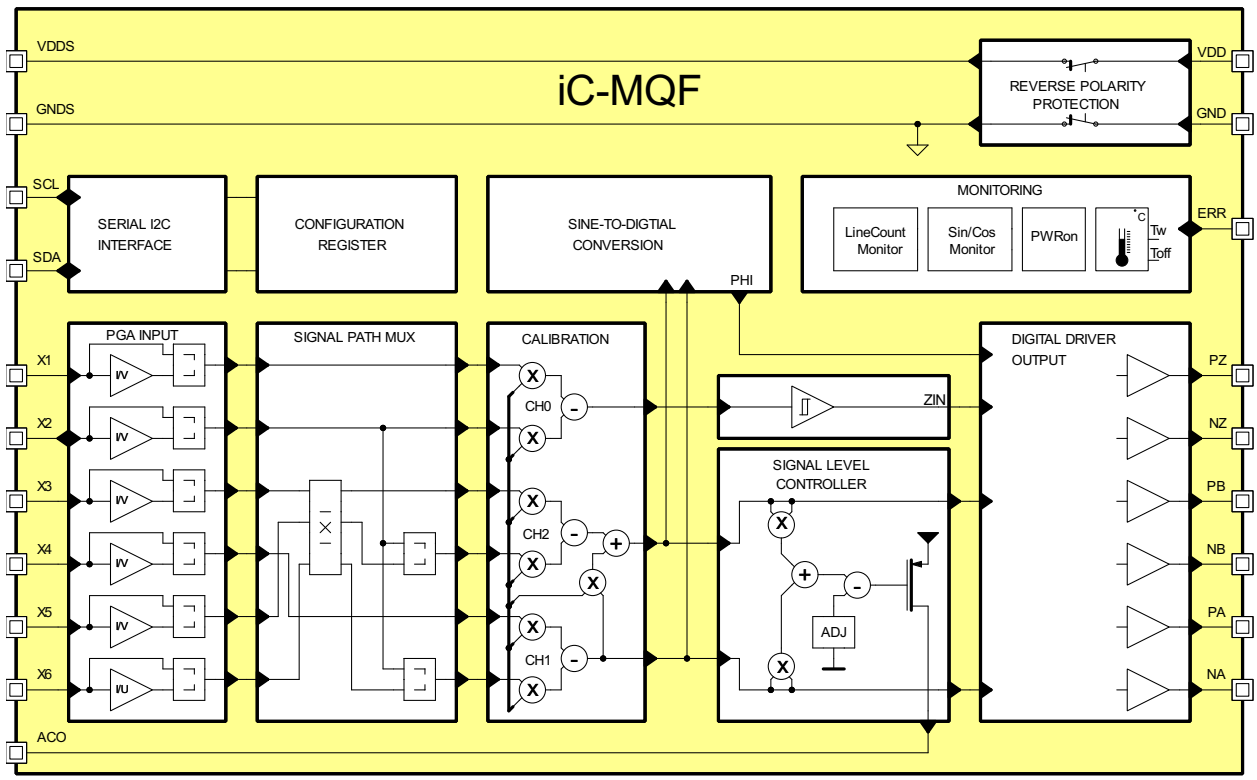
- Optical and magnetic position sensors
- Linear scales
- High-resolution angle sensing

PACKAGES



TSSOP20

BLOCK DIAGRAM



DESCRIPTION

Interpolator iC-MQF is a non-linear A/D converter which digitizes sine/cosine sensor signals using a count-safe tracking conversion principle with selectable resolution and hysteresis. The angle resolution per sine period can be set using SELRES; up to 4000 angle steps are possible (see page 27).

The angle position is output incrementally by differential RS422 drivers as an encoder quadrature signal with a zero pulse or, if selected, as a counter signal for devices compatible with 74HC191 or 74HC193.

The zero pulse is generated electronically when an enable has been set by the X1/X2 inputs. This pulse can be configured extensively: both in its relative position to the input signal with regard to the logic gating with A and/or B and in its width from 90° to 360° (1/4 to 1 T).

A preselectable minimum transition distance ensures glitch-free output signals and prevents counting errors which in turn boosts the noise immunity of the position encoder.

Programmable instrumentation amplifiers with selectable gain levels allow differential or single-ended, referenced input signals; a external reference can be used via input X2 as reference voltage for the offset correction.

The modes of operation differentiate between high impedance (V modes) and low impedance (I modes). This adaptation of the iC to voltage or current signals enables MR sensor bridges or photosensors to be directly connected up to the device. The optical scanning of low resolution code discs is also supported by the reference function of input X2; these discs do not evaluate tracks differentially but in comparison with a reference photodiode.

The integrated signal conditioning unit allows signal amplitudes and offset voltages to be calibrated accurately and any phase error between the sine and cosine signals to be corrected. The channel for the zero signal can be configured separately.

A control signal is generated from the conditioned signals which can track the transmitting LED of optical encoders via the integrated 50 mA driver stage (output ACO). If MR sensors are connected this driver stage can also track the power supply of the measuring bridges. By tracking the sensor energy supply any temperature and aging effects are compensated for, the input signals stabilized and the exact calibration of the input signals is maintained. This enables a constant accuracy of the interpolation circuit across the entire operating temperature range.

If control limits are reached, these can be indicated at the maskable error pin ERR. Faults such as overdrive, wire breakage, short circuiting, dirt or aging, for example, can be logged.

iC-MQF includes extensive self-test and system diagnosis functions which check whether the sensor is working properly or not. For all error events the user can select whether the fault is indicated at the pin ERR or whether the outputs should shutdown. At the same time errors can be stored in the EEPROM to enable failures to be diagnosed at a later stage. For encoder applications the line count of the code disc, the sensor signal regarding signal level and frequency and the operating temperature can be monitored, for example, the latter using an adjustable on-chip sensor.

Display error pin ERR is bidirectional; a system fault recognized externally can be recorded and also registered in the error memory.

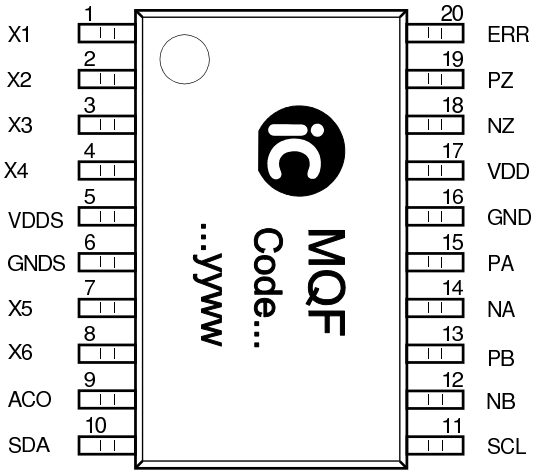
iC-MQF is protected against reverse polarity and offers its monitored supply voltage to the external circuit, thus extending the protection to the system (for load currents up to 20 mA). Reverse polarity protection also covers the short-circuit-proof line drivers so that an unintentional faulty wiring during initial operation is tolerated.

On being activated the device configuration is loaded via the serial configuration interface from an external EEPROM and verified with a CRC. A microcontroller can also configure iC-MQF; the implemented interface is multimaster-competent and allows direct RAM access.

CONTENTS

PACKAGING INFORMATION

PIN CONFIGURATION TSSOP20



PIN FUNCTIONS

No.	Name	Function
1	X1	Signal Input 1 (Index +)
2	X2	Signal Input 2 (Index -)
3	X3	Signal Input 3
4	X4	Signal Input 4
5	VDDS[1)]	Switched Supply Output and Internal Analog Supply Voltage (reverse polarity proof, load 20 mA max.)
6	GNDS[1)]	Switched Ground (reverse polarity proof)
7	X5	Signal Input 5
8	X6	Signal Input 6
9	ACO	Signal Level Controller, high-side current source output
10	SDA	Serial Configuration Interface, data line
11	SCL	Serial Configuration Interface, clock line
12	NB	Incremental Output B-
13	PB	Incremental Output B+
14	NA	Incremental Output A-
15	PA	Incremental Output A+
16	GND	Ground
17	VDD	+4.3...5.5 V Supply Voltage
18	NZ	Incremental Output Z-
19	PZ	Incremental Output Z+
20	ERR	Error Signal (In/Out) / Test Mode Trigger Input

1) It is advisable to connect a bypass capacitor of at least 100 nF close to the chip's analog supply terminals.

ABSOLUTE MAXIMUM RATINGS

Beyond these values damage may occur; device operation is not guaranteed.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	V()	Voltage at VDD, PA, NA, PB, NB, PZ, NZ, SCL, SDA, ACO		-6	6	V
G002	V()	Voltage at ERR		-6	8	V
G003	V()	Pin-to-Pin Voltage			6	V
G004	V()	Voltage at X1...X6, SCL, SDA		-0.3	VDDS + 0.3	V
G005	I(VDD)	Current in VDD		-20	400	mA
G006	I()	Current in VDDS, GNDS		-50	50	mA
G007	I()	Current in X1...X6, SCL, SDA, ERR		-20	20	mA
G008	I()	Current in PA, NA, PB, NB, PZ, NZ		-100	100	mA
G009	I(ACO)	Current in ACO		-100	20	mA
G010	Vd()	ESD Susceptibility at all pins	HBM 100 pF discharged through 1.5 kΩ		2	kV
G011	Ptot	Permissible Power Dissipation			300	mW
G012	Tj	Junction Temperature		-40	150	°C
G013	Ts	Storage Temperature		-40	150	°C

THERMAL DATA

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range		-40		100	°C
T02	Rthja	Thermal Resistance Chip to Ambient			80		K/W

All voltages are referenced to pin GNDS unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 4.3 ... 5.5 V, Tj = -40 °C ... 125 °C, IBN calibrated to 200 µA, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device							
001	V(VDD)	Permissible Supply Voltage	Load current I(VDDS) to 10 mA Load current I(VDDS) to 20 mA	4.3 4.5		5.5 5.5	V V
002	I(VDD)	Supply Current	Tj = -40...125 °C, no load Tj = 27 °C, no load		 18	25	mA mA
003	I(VDDS)	Permissible Load Current VDDS		-20		0	mA
004	Vcz()hi	Clamp-Voltage hi at all pins				11	V
005	Vc()hi	Clamp-Voltage hi at Inputs SCL, SDA	Vc()hi = V() - V(VDD), I() = 1 mA	0.4		1.5	V
006	Vc()hi	Clamp-Voltage hi at Inputs X1...X6	Vc()hi = V() - V(VDD), I() = 4 mA	0.3		1.2	V
007	Vc()lo	Clamp-Voltage lo at all pins	I() = -4 mA	-1.2		-0.3	V
008	Irev(VDD)	Reverse-Polarity Current VDD vs. GND	V(VDD) = −5.5V...−4.3 V	-1		1	mA
Signal Conditioning, Inputs X1...X6 (CH1, CH2: i = 12, CH0: i = 0)							
101	Vin()sig	Permissible Input Voltage Range	Ri() = 0x01 Ri() = 0x09	0.75 0		VDDS − 1.5 VDDS	V V
102	Iin()sig	Permissible Input Current Range	Ri(0) = 0; BIASi = 0 Ri(0) = 0; BIASi = 1	-300 10		-10 300	µA µA
103	Iin()	Input Current	Ri() = 0x01	-0.5		0.5	µA
104	Vout(X2)	Output Voltage at X2	MUX = 0x20...0x2F, I(X2) = 0, referenced to VREFin12	95	100	105	%
105	Vin(X2)	Permissible Input Voltage at X2	MUX = 0x30...0x3F	0.5		VDDS − 2	V
106	Rin(X2)	Input Resistance at X2	MUX = 0x30...0x3F, R0(3:0) = 0x01, R12(3:0) = 0x01	20	27	35	kΩ
107	Rin()	Input Resistance vs. VREFin	Tj = 27 °C; Ri(3:0) = 0x09 Ri(3:0) = 0x00 Ri(3:0) = 0x02 Ri(3:0) = 0x04 Ri(3:0) = 0x06	 16 1.1 1.6 2.2 3.2	 20 1.6 2.3 3.2 4.6	 24 2.1 3.0 4.2 6.0	 kΩ kΩ kΩ kΩ kΩ
108	TC(Rin)	Temperature Coefficient of Rin			0.15		%/K
109	VREFin()	Reference Voltages VREFin0, VREFin12	Ri(0) = 0, BIASi = 1 Ri(0) = 0, BIASi = 0	1.35 2.25	1.5 2.5	1.65 2.75	V V
110	G0, G12	Selectable Gain Factors	MODE = 0x05, Ri(3) = 0, GRi and GFi = 0x0 MODE = 0x05, Ri(3) = 0, GRi and GFi = max. MODE = 0x05, Ri(3) = 1, GRi and GFi = 0x0 MODE = 0x05, Ri(3) = 1, GRi and GFi = max.		6 300 1.5 75		
111	Gdiff	Relative Gain Ratio CH1 vs. CH2	GF2 = 0x10, GF1 = 0x0 GF2 = 0x10, GF1 = 0x7FF		39 255		% %
112	ΔG	Step Width Of Fine Gain Adjustment	for CH0 for CH1 for CH2		1.06 1.0009 1.06		
113	INL(Gi)	Integral Linearity Error of Gain Adjustment		-1.06		1.06	
114	Vin()diff	Recommended Differential Input Voltage	Vin()diff = V(PCHx) - V(NCHx); Ri(3) = 0 Ri(3) = 1	 20 80		 1000 4000	 mVpp mVpp
115	Vin()os	Input Offset Voltage	referred to side of input		25		µV
116	VOScal	Offset Calibration Range	referenced to the selected source (VOS0 resp. VOS12), mode *Calibration 2*; ORi = 00 ORi = 01 ORi = 10 ORi = 11		 ±100 ±200 ±600 ±1200		 %V() %V() %V() %V()

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 4.3 ... 5.5 V, Tj = -40 °C ... 125 °C, IBN calibrated to 200 µA, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
117	ΔOF0	CH0 Offset Calibration Step Width	referenced to the selected source VOS0; OR0 = 0x0		3.2		%
118	ΔOF12	CH1/2 Offset Calibration Step Width	referenced to the selected source VOS12; OR12 = 0x0		0.79		%
119	INL(OFi)	Integral Linearity Error of Offset Calibration	limited test coverage (guaranteed by design)	-5		5	LSB
120	PHI12	Phase Error Calibration Range	CH1 vs. CH2		±10.4		°
121	ΔPHI12	Phase Error Calibration Step Width			0.02		°
122	INL(PHI12)	Integral Linearity Error of Phase Calibration	limited test coverage (guaranteed by design)	-0.8		0.8	°
123	fin()	Permissible Maximum Input Freq.	analog signal path	200			kHz
Sine-To-Digital Conversion							
201	AAabs	Absolute Angle Accuracy	referenced to 360° input signal, ideal waveform, quasi static signals, adjusted signal conditioning, SELHYS = 0		0.13		°
202	AArel	Relative Angle Accuracy	referenced to output period T (see Fig. 1), ideal waveform, quasi static signals; at 4 edges per period at 200 edges per period at 500 edges per period at 1000 edges per period at 2000 edges per period at 4000 edges per period		 1.7 3.5 7 14 28	 10 10 10 15 30 50	 % % % % % %
203	AAR	Repeatability	see 201; VDD = const., Tj = const.		0.1		°
204	fin()max	Maximum Input Frequency for Sine-To-Digital Conversion	MTD = 0x01, IPF < 10; refer to Figure 2 for dependencies			200	kHz
Line Driver Outputs PA, NA, PB, NB, PZ, NZ							
501	Vs()hi	Saturation Voltage hi	Vs()hi = VDD - V(); SIK(1:0) = 00, I() = -1.2 mA SIK(1:0) = 01, I() = -4 mA SIK(1:0) = 10, I() = -20 mA SIK(1:0) = 11, I() = -50 mA			 200 200 400 700	 mV mV mV mV
502	Vs()lo	Saturation Voltage lo	SIK(1:0) = 00, I() = 1.2 mA SIK(1:0) = 01, I() = 4 mA SIK(1:0) = 10, I() = 20 mA SIK(1:0) = 11, I() = 50 mA			200 200 400 700	mV mV mV mV
503	Isc()hi	Short-Circuit Current hi	V() = 0 V; SIK(1:0) = 00 SIK(1:0) = 01 SIK(1:0) = 10 SIK(1:0) = 11	 -4 -12 -60 -150		 -1.2 -4 -20 -50	 mA mA mA mA
504	Isc()lo	Short-Circuit Current lo	V() = VDD; SIK(1:0) = 00 SIK(1:0) = 01 SIK(1:0) = 10 SIK(1:0) = 11	 1.2 4 20 50		 4 12 60 150	 mA mA mA mA
505	tr()	Rise Time	RL = 100 Ω to GND; SSR(1:0) = 00 SSR(1:0) = 01 SSR(1:0) = 10 SSR(1:0) = 11	 5 5 20 50		 20 40 140 350	 ns ns ns ns
506	tf()	Fall Time	RL = 100 Ω to VDD; SSR(1:0) = 00 SSR(1:0) = 01 SSR(1:0) = 10 SSR(1:0) = 11	 5 5 30 50		 20 40 140 350	 ns ns ns ns
507	Ilk()tri	Leakage Current	TRIHL(1:0) = 11 (tristate)		20	100	µA
508	Ilk()rev	Leakage Current	reversed supply voltage		100		µA
509	Rin()cal	Test Signal Source Impedance	Op. modes *Calibration 1, 2, 3*		2.5	4	kΩ

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 4.3 ... 5.5 V, Tj = -40 °C ... 125 °C, IBN calibrated to 200 µA, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
510	I()cal	Permissible Test Signal Load	Op. modes *Calibration 1, 2, 3*	-3		3	µA
511	tclk()lo	Clock Signal Low-Pulse Duration for CP, CPD, CPU	Op. mode *Mode 191/193*; MTD = 0x03 MTD = 0x04 MTD = 0x05 MTD = 0x06 MTD = 0x07 MTD = 0x08 MTD = 0x09 MTD = 0x0A MTD = 0x0B MTD = 0x0C MTD = 0x0D MTD = 0x0E MTD = 0x0F		 50 62.5 75 87.5 100 150 200 300 400 500 600 700 800		 ns ns ns ns ns ns ns ns ns ns ns ns ns
512	tw()hi	Duty Cycle	referenced to output period T, see Figure 1		50		%
513	t_{AB}	Phase Shift A vs. B	see Figure 1		25		%
514	t_{MTD}	Minimum Phase Distance	edge to edge, see Figure 1, CFGOSZ calibrated; MTD = 0x01 MTD = 0x02 MTD = 0x03 MTD = 0x04 MTD = 0x05 MTD = 0x06 MTD = 0x07 MTD = 0x08 MTD = 0x09 MTD = 0x0A MTD = 0x0B MTD = 0x0C MTD = 0x0D MTD = 0x0E MTD = 0x0F	 45 65 90 110 130 150 175 260 345 515 685 860 1030 1200 1370		 75 115 135 170 200 230 260 390 520 780 1040 1300 1560 1820 2080	 ns ns ns ns ns ns ns ns ns ns ns ns ns ns ns
515	Δt_{MTD}	Minimum Phase Distance Variation	VDD = 4.3...5.5 V, Tj = 27 °C, variation vs. VDD = 5 V; VDD = 5 V, Tj = -40...125 °C, variation vs. Tj = 27 °C;	-10 -5		10 15	% %
Signal Level Controller ACO							
601	Vs()hi	Saturation Voltage hi	Vs()hi = VDD - V(), ACOT(1:0) = 0x2, ACOS(4:0) = 0x1F; ACOR(1:0) = 0x0, I() = -5 mA ACOR(1:0) = 0x1, I() = -10 mA ACOR(1:0) = 0x2, I() = -25 mA ACOR(1:0) = 0x3, I() = -50 mA			 1 1 1 1.2	 V V V V
602	Isc()hi	Short-Circuit Current hi	V() = 0 ... VDD - Vs()hi, ACOT(1:0) = 0x2, ACOS(4:0) = 0x1F; ACOR(1:0) = 0x0 ACOR(1:0) = 0x1 ACOR(1:0) = 0x2 ACOR(1:0) = 0x3	 -10 -20 -50 -100		 -5 -10 -25 -50	 mA mA mA mA
603	It()min	Control Range Monitoring 1: lower limit	referenced to range ACOR(1:0)		3		%Isc
604	It()max	Control Range Monitoring 2: upper limit	referenced to range ACOR(1:0)		90		%Isc
605	Vt()min	Signal Level Monitoring 1: lower limit	referenced to Vscq()		40		%Vpp
606	Vt()max	Signal Level Monitoring 2: upper limit	referenced to Vscq()		130		%Vpp

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 4.3 ... 5.5 V, Tj = -40 °C ... 125 °C, IBN calibrated to 200 µA, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Bias Current Source and Reference Voltages							
801	IBN	Bias Current Source	*Calibration 1*, I(NB) vs. VDDS; CFGIBN = 0x0 CFGIBN = 0xF IBN calibrated at Tj = 25 °C	 110 180	 200	 370 220	 µA µA µA
802	VBG	Internal Bandgap Reference		1.2	1.25	1.3	V
803	VPAH	Reference Voltage		45	50	55	%VDDS
804	V05	Reference Voltage V05		450	500	550	mV
805	V025	Reference Voltage V025			50		%V05
Power-Down-Reset							
901	VDDon	Turn-on Threshold VDD, Power-Up-Enable	increasing voltage at VDD	3.6	4.0	4.3	V
902	VDDoff	Turn-off Threshold VDD, Power-Down-Reset	decreasing voltage at VDD	3.0	3.5	3.8	V
903	VDDhys	Hysteresis		0.4			V
Error Signal Input/Output, Pin ERR							
B01	Vs()lo	Saturation Voltage lo	versus GND, I() = 4 mA			0.4	V
B02	Isc()lo	Short-Circuit Current lo	versus GND, V(ERR) ≤ VDD	4	5	8	mA
B03	Isc()	Low-Side Current Source For Data Output	versus GND, V(ERR) > VTMon L state Z state		 2 0		 mA mA
B04	Vt()hi	Input Threshold Voltage hi	versus GND			2	V
B05	Vt()lo	Input Threshold Voltage lo	versus GND	0.8			V
B06	Vt()hys	Input Hysteresis	Vt()hys = Vt()hi − Vt()lo	300	500		mV
B07	Ipu()	Input-Pull-Up-Current	V() = 0...VDD − 1 V, EPU = 1	-400	-300	-200	µA
B08	Vpu()	Pull-Up-Voltage	Vpu() = VDD − V(), I() = -5 µA, EPU = 1			0.4	V
B09	VTMon	Test Mode Turn-on Threshold	increasing voltage at ERR			VDD + 2	V
B10	VTMoff	Test Mode Turn-off Threshold	decreasing voltage at ERR	VDD + 0.5			V
B11	VTMhys	Test Mode Threshold Hysteresis	VTMhys = VTMon − VTMoff	0.15	0.3		V
B12	fclk()	Data Output Signal Frequency	ENFAST = 0 ENFAST = 1	120 480	160 640	200 800	kHz kHz
B13	tp(ERR)in	Process Delay for System Error Message at ERR	upon power up (VDD > VDDon)		10		ms
Reverse Polarity Protection and Supply Switches VDDS, GNDS							
C01	Vs()	Saturation Voltage vs. VDD	Vs(VDDS) = VDD − V(VDDS); I(VDDS) = -10...0 mA I(VDDS) = -20...-10 mA			 150 250	 mV mV
C02	Vs()	Saturation Voltage vs. GND	Vs(GNDS) = V(GNDS) − GND; I(GNDS) = 0...10 mA I(GNDS) = 10...20 mA			 150 200	 mV mV
C03	C()	Backup Capacitor Analog Supply VDDS vs. GNDS		100			nF

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 4.3 ... 5.5 V, Tj = -40 °C ... 125 °C, IBN calibrated to 200 µA, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Serial Configuration Interface SCL, SDA							
D01	Vs()lo	Saturation Voltage lo	I() = 4 mA			400	mV
D02	Isc()lo	Short-Circuit Current lo		4		75	mA
D03	Vt()hi	Input Threshold Voltage hi				2	V
D04	Vt()lo	Input Threshold Voltage lo		0.8			V
D05	Vt()hys	Input Hysteresis	Vt()hys = Vt()hi – Vt()lo	300	500		mV
D06	Ipu()	Input Pull-Up Current	V() = 0...VDDS – 1 V	-600	-300	-60	µA
D07	Vpu()	Pull-Up Voltage	Vpu() = VDDS – V(), I() = -5 µA			0.4	V
D08	fclk()	Clock Frequency at SCL	ENFAST = 0 ENFAST = 1	60 240	80 320	100 400	kHz kHz
D09	tbusy()cfg	Duration of Startup Configuration	IBN not calibrated, EEPROM access without read failure, time to outputs operational; ENFAST = 0 ENFAST = 1		 36 24	 48 34	 ms ms
D10	tbusy()err	End Of I2C Communication; Time Until I2C Slave Is Enabled	IBN not calibrated; V(SDA) = 0V V(SCL) = 0V or arbitration lost no EEPROM CRC ERROR		4 indef. 45 95	12 135 285	ms ms ms ms
D11	tp()	Start Of Master Activity On I2C Protocol Error	SCL without clock signal: V(SCL) = constant; IBN not calibrated IBN calibrated to 200 µA	 25 64	 80 80	 240 150	 µs µs
Temperature Monitoring							
E01	VTs	Temperature Sensor Voltage	VTs() = VDDS – V(PA), *Calibration 3*, without load; Tj = -40 °C Tj = 27 °C Tj = 100 °C	 740 620 460	 770 650 520	 790 670 540	 mV mV mV
E02	TCs	Temp. Co. Temperature Sensor Voltage			-1.8		mV/K
E03	VTth	Temperature Warning Activation Threshold	VTth() = VDDS - V(NA), Tj = 27 °C, *Calibration 3*, without load; CFGTA(3:0) = 0x0 CFGTA(3:0) = 0xF	 260 470	 310 550	 360 630	 mV mV
E04	TCth	Temp. Co. Temperature Warning Activation Threshold			0.06		%/K
E05	Tw	Warning Temperature	CFGTA(3:0) = 0x0 CFGTA(3:0) = 0xF	125	140 65	 80	°C °C
E06	Thys	Warning Temperature Hysteresis	80 °C < Tj < 125 °C	10	15	25	°C
E07	ΔT	Relative Shutdown Temperature	ΔT = Toff – Tw	5	15	25	°C

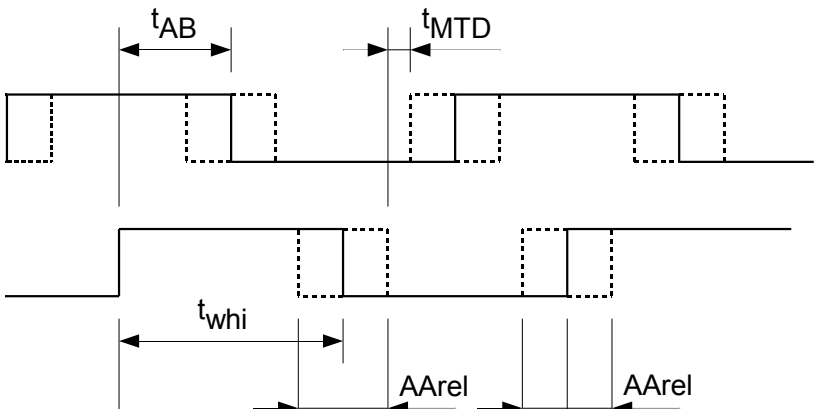


Figure 1: Definition of relative angle error and minimum phase distance.

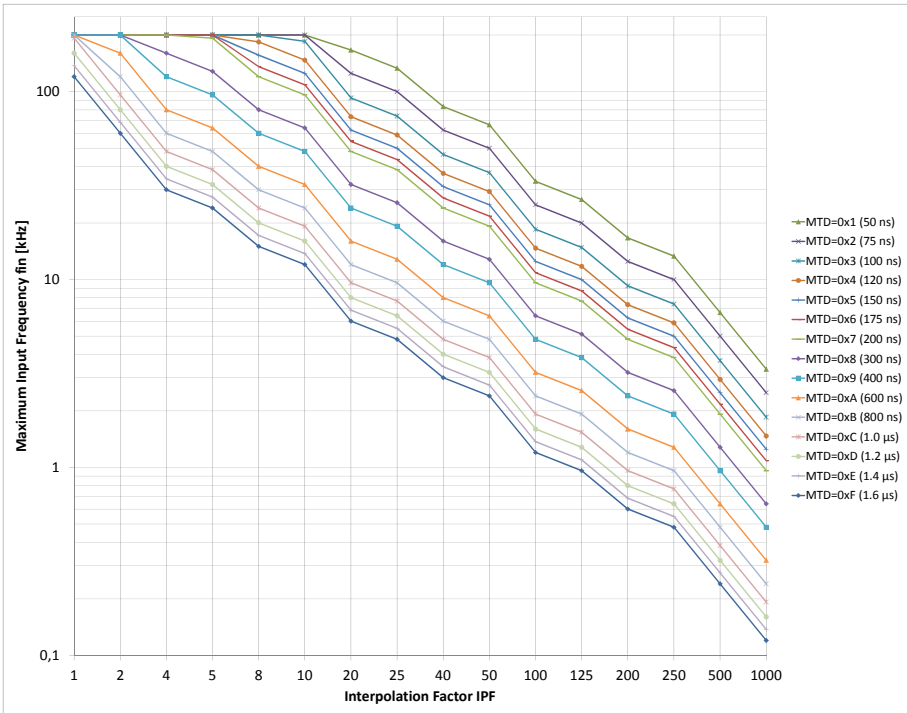


Figure 2: Maximum input frequency depending on interpolation factor.

PROGRAMMING

REGISTER MAP

Register Map								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Calibration								
0x00	0	0	0	ENFAST	CFGIBN(3:0)			
0x01	0	0	0	CFGTA(4:0)				
Operating Mode								
0x02	END**	ENSL	0	ENZFF	MODE(3:0)			
Input Configuration								
0x03	ENF	MUX(6:0)						
0x04	0	BIAS0	VOS0(1:0)		R0(3:0)			
0x05	0	BIAS12	VOS12(1:0)		R12(3:0)			
0x06	1	1	0	1	0	0	0	0
Signal Conditioning CH0								
0x07	0	GR0(2:0)			0	0	OR0(1:0)	
0x08	0	0	0	GF0(4:0)				
0x09	0	0	OF0(5:0)					
Signal Conditioning CH1, CH2								
0x0A	GF1(3:0)				0	GR12(2:0)		
0x0B	0	GF1(10:4)						
0x0C	0	0	0	GF2(4:0)				
0x0D	VDC1(7:0)							
0x0E	VDC2(3:0)				0	0	VDC1(9:8)	
0x0F	0	0	VDC2(9:4)					
0x10	OF1(3:0)				OR2(1:0)		OR1(1:0)	
0x11	0	OF1(10:4)						
0x12	OF2(7:0)							
0x13	PH12(3:0)				0	OF2(10:8)		
0x14	0	0	PH12(9:4)					
Signal Level Controller								
0x15	ACOR(1:0)		ACOS(4:0)					0
0x16	0	0	0	0	0	0	ACOT(1:0)	
Error Monitoring and Alarm Output								
0x17	EMASKA(7:0)							
0x18	0	EMTD(2:0)			0	0	EMASKA(9:8)	
0x19	EMASKO(7:0)**							
0x1A	0	PDMODE	EPU	EPH	0	0	EMASKO(9:8)	
0x1B	EMASKE(7:0)**							
0x1C	0	EMODE(2:0)			0	0	EMASKE(9:8)**	
Zero Signal Output								
0x1D	CFGABZ(7:0)							
0x1E	CFGZPOS(7:0)							
Sine-To-Digital-Conversion, Minimum Phase Distance								
0x1F	MTD(3:0)				SELHYS(3:0)			
0x20	SELRES(7:0)							
0x21	0	SELRES(14:8)						

Register Map								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Output Driver Settings								
0x22	0	0	SIK(1:0)		SSR(1:0)		TRIHL(1:0)	
Line Counter								
0x23	LINECNT(7:0)							
0x24	0	0	LINECNT(13:8)					
Sine-To-Digital-Conversion, Calibration								
0x25	0	0	0	0	0	CFGOSZ(2:0)		
Reserved								
0x26	0	0	0	0	0	0	0	0
0x27	0	0	0	0	0	0	0	0
0x28	0	0	0	0	0	0	0	0
0x29	free for OEM data							
0x2A	free for OEM data							
0x2B	free for OEM data							
0x2C	free for OEM data							
0x2D	free for OEM data							
0x2E	free for OEM data							
Check Sum								
0x2F	CHKSUM(7:0) of EEPROM data [CHPREL(7:0), refer to Table 7]							
Error Register								
0x30	ERR1(7:0)							
0x31	ERR2(5:0)						ERR1(9:8)	
0x32	ERR3(3:0)				ERR2(9:6)			
0x33	0	0	ERR3(9:4)					
Notes	The device RAM initially contains random data following power-on. **) Mandatory programming of EEPROM: END = 1, EMASKO(7, 6) = 0, EMASKE(8, 7, 6) = 0.							

Table 4: Register layout (EEPROM)

SERIAL CONFIGURATION INTERFACE

The serial configuration interface consists of the two pins SCL and SDA and enables read and write access to an EEPROM with an I²C interface. The readout clock rate can be selected using ENFAST.

ENFAST	Adr 0x00, bit 4
Code	Function
0	Regular clock rate, f(SCL) approx. 80 kHz
1	High clock rate, f(SCL) approx. 320 kHz
Notes	For in-circuit programming bus lines SCL and SDA require pull-up resistors. For line capacitances to 170 pF, adequate values are: 4.7 kΩ with clock frequency 80 kHz 2 kΩ with clock frequency 320 kHz The pull-up resistors may not be less than 1.5 kΩ. To separate the signals a ground line between SCL and SDA is recommended. iC-MQF requires a supply voltage during EEPROM programming (5 V to VDD).

Table 5: I²C Fast Mode

Once the supply has been switched on, the iC-MQF outputs are high impedance (tristate) until a valid configuration is read out from the EEPROM using device ID 0x50.

Bit errors in the 0x00 to 0x2F memory section are pinpointed by the CRC deposited in register CHKSUM(7:0) (address 0x2F in the EEPROM; the CRC polynomial used is "'1 0001 1101"' with a start value of "1").

If the configuration data is not confirmed by the CRC, the readin process is repeated. If no valid configuration data is available after a fourth readin, iC-MQF terminates EEPROM access and switches to I²C slave mode. This switch takes place after 150 ms at the latest (see Electrical Characteristics, D11), for example if no EEPROM is connected.

Bit ENSL decides (for devices loading a valid configuration from the EEPROM register) whether the I²C slave function is enabled or not.

ENSL	Adr 0x02, bit 6
Code	Function
0	Normal operation
1	I²C Slave Mode Enable (Device ID 0x55)

Table 6: I²C Slave Mode

Example of CRC Calculation Routine

```
unsigned char ucDataStream = 0;
int iCRCPoly = 0x11D;
unsigned char ucCRC=0;
int i = 0;

ucCRC = 1; // start value !!!
for (iReg = 0; iReg<47; iReg ++)
{
  ucDataStream = ucGetValue(iReg);
  for (i=0; i<=7; i++) {
    if ((ucCRC & 0x80) != (ucDataStream & 0x80))
      ucCRC = (ucCRC << 1) ^ iCRCPoly;
    else
      ucCRC = (ucCRC << 1);
    ucDataStream = ucDataStream << 1;
  }
}
```

EEPROM Selection

The following minimal requirements must be fulfilled:

- Operation from 3.3 to 5 V, I²C interface
- At least 512 bits, 64x8
  (address range used is 0x00 to 0x3F)
- Support of *Page Write* with *Pages* of at least 4 bytes. Otherwise, errors can not be saved to the EEPROM (EMASKE = 0x0).
- Device ID 0x50 "1010 000", no occupation of 0x55 (A2...A0 = 0). Otherwise, iC-MQF can not be accessed via 0x55 in I²C slave mode.

Recommended devices: Atmel AT24C01, ST M24C01, ST M24C02 (2K), ROHM BR24L01A-W, BR24L02-W

I²C Slave Mode (ENSL = 1)

In this mode iC-MQF behaves like an I²C slave with the device ID 0x55 and the configuration interface permits write and read accesses to iC-MQF's internal registers.

For chip release verification purposes an identification value is stored under ROM address 0x2F; a write access to this address is not permitted.

CHPREL	Adr 0x2F, bit 7:0 (ROM)
Code	Chip Release
0x22	iC-MQ F2
0x23	iC-MQ F3

Table 7: Chip Release

END	Adr 0x02, bit 7
Code	Function
0	Standby: Sin/D converter and line driver disabled (configuration changes allowed, see Table 10)
1	Enable Device: Restart of Sin/D conversion, line driver active (configuration data must be valid)
Notes	END is evaluated only during I²C slave mode. Write access changes the function. Read access does not return the chip's state. Program END = 1 to EEPROM.

Table 8: Configuration Enable

The registers 0x0 to 0x2E must be initialized with correct values before enabling iC-MQF. This can be done through the I²C slave interface if iC-MQF is used without EEPROM or if the EEPROM content is invalid. Initially, END (bit 7 of address 0x02) must be set to zero, then all registers must be configured. Finally, set END to one without changing other bits of address 0x02 to enable the device.

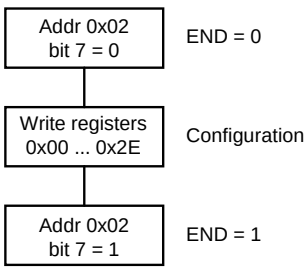


Figure 3: Programming via I²C. END is altered by changing only bit 7 of address 0x02 and leaving bits 6:0 unchanged.

Intermediate error information buffer (Addr. 0x40-0x43)

The intermediate error information buffer is initialized whenever iC-MQF is enabled (END set to 1): ERR1 and ERR3 data is copied from RAM Addr. 0x30-0x33, and ERR2 data is initialized with 0.

The intermediate error information is modified based on EMASKE and occurring errors. (See section *Error Logging* on page 31.)

The data of the intermediate error information buffer is invalid after an EEPROM write access failed. In this case END must be toggled (set to 0, then set to 1) before accessing the intermediate error information buffer.

Register	Read access via I²C slave mode (ENSL = 1)
RAM Addr	Content
0x00-0x25	Configuration data (see EEPROM addresses 0x00-0x25)
0x26-0x28	Not available*
0x29-0x2E	Configuration data (see EEPROM addresses 0x29-0x2E)
0x2F	Chip release CHPREL(7:0)
0x30-0x33	Configuration data (see EEPROM addresses 0x30-0x33)
0x34-0x38	Not available
0x39-0x3E	Configuration data (see EEPROM addresses 0x29-0x2E)
0x3F	Chip release CHPREL(7:0)
0x40-0x43	Intermediate error information buffer
0x44-0x7F	Not available
Notes	*) The EEPROM addresses 0x26-0x28 are not available in iC-MQF RAM.

Table 9: RAM Read Access

Register	Write access via I²C slave mode (ENSL = 1)
RAM Addr	Access and conditions
0x00	Changes permitted (wrong entries for CFGIBN can limit functions)
0x01	Changes permitted
0x02	Changes to bits 6:0 are permitted only during standby (END = 0, ie. bit 7); Restarting Sin/D conversion by changing END (bit 7) is permitted only with no changes of operating mode (bits 6:0 remain as set)
0x03-0x16	Changes permitted, no restrictions
0x1B-0x25	Changes are permitted during standby (END = 0)
0x26-0x28	Not available
0x29-0x2E	Changes permitted, no restrictions
0x2F	No write access permitted
0x30-0x33	Changes permitted during standby (END = 0)
0x34-0x43	No write access permitted
0x44-0x7F	Not available

Table 10: RAM Write Access

BIAS CURRENT SOURCE AND TEMPERATURE SENSOR CALIBRATION

Bias Current

The calibration of the bias current source in operation mode *Calibration 1* (see Table 13) is prerequisite for adherence to the given electrical characteristics and also instrumental in the determination of the chip timing (e.g. clock frequency at SCL). The IBN bias current is measured by connecting pin VDDS and pin NB with a 10 kΩ resistor. The setpoint is 200 µA which is equivalent to a voltage drop of 2 V.

Notice: The measurement delivers a false reading when outputs are tristate (due to a configuration error after cycling power, for instance).

CFGIBN	Adr 0x00, bit 3:0		
Code k	$IBN \sim \frac{31}{39-k}$	Code k	$IBN \sim \frac{31}{39-k}$
0x0	79 %	0x8	100 %
0x1	81 %	0x9	103 %
0x2	84 %	0xA	107 %
0x3	86 %	0xB	111 %
0x4	88 %	0xC	115 %
0x5	91 %	0xD	119 %
0x6	94 %	0xE	124 %
0x7	97 %	0xF	129 %

Table 11: Bias Current

Temperature Sensor

The temperature monitoring is calibrated in operating mode *Calibration 3*.

The voltage VTs, at which the warning message is generated, is determined first. A voltage ramp from VDDS towards GNDS is applied to pin PA until pin ERR displays the warning message. The following settings are required for this measurement: EMASKA = 0x20, EMTD = 0x00 and EPH = 0x00.

The signal at pin ERR switches from tristate to low (on reaching the warning threshold VTs) and then from low to tristate (on overshooting the threshold of the overtemperature self protection which is not relevant to calibration). To avoid confusion a clear change of state (from low to high) should be generated with the help of an external pull-up resistor at pin ERR.

Example: VTs(T_1) is ca. 650 mV, measured from VDDS versus PA, with T_1 = 25 °C; -

The necessary reference voltage VTth(T_1) is then calculated. The required warning temperature T_2, temperature coefficients TCs and TCth (see Electrical Characteristics, Section E) and measurement value VTs(T_1) are entered into this calculation:

$$VTth(T_1) = \frac{VTs(T_1) + TCs \cdot (T_2 - T_1)}{1 + TCth \cdot (T_2 - T_1)}$$

Example: For T_2 = T_1 + 100 K VTth(T_1) must be programmed to 443 mV.

Reference voltage VTth(T_1) is provided for a high impedance measurement (10 MΩ) at output pin NA (measurement against VDDS) and must be set to the calculated value by programming CFGTA(3:0).

Example: Altering VTth(T_1) from 310 mV (measured with CFGTA(3:0)= 0x0) to 443 mV is equivalent to 143 %, the closest value for CFGTA is 0x9;

CFGTA	Adr 0x01, bit 4:0		
Code k	$VTth \sim \frac{65+3k}{65}$	Code k	$VTth \sim \frac{65+3k}{65}$
0x0	100 %	0x8	137 %
0x1	105 %	0x9	142 %
0x2	109 %	0xA	146 %
0x3	114 %	0xB	151 %
0x4	118 %	0xC	155 %
0x5	123 %	0xD	160 %
0x6	128 %	0xE	165 %
0x7	132 %	0xF	169 %
0x10-0x1F	reserved		
Notes	With CFGTA = 0xF Toff is 80 °C typ., with CFGTA = 0x0 Toff is 155 °C typ.		

Table 12: Temperature Monitoring

OPERATING MODES

iC-MQF has various modes of operation, for which the functions of outputs PA, NA, PB, NB, PZ, NZ and ERR are altered.

Two operating modes can be selected for the output of the angle position in normal operation. *Mode 191/193* provides control signals for devices compatible with 74HC191 or 74HC193, whereas in *Mode ABZ* the angle position is output incrementally as an encoder quadrature signal with a zero pulse. Only in these modes are the line drivers and the reverse polarity protection feature active.

In order to condition the input signals and to calibrate and test iC-MQF *Calibration* and *Test* modes are available. Digital and analog test signals are provided; the latter must always be measured at high load impedance.

MODE(3:0)		Addr. 0x02; bit 3:0						
Code	Operating Mode	Pin PA	Pin NA	Pin PB	Pin NB	Pin PZ	Pin NZ	Pin ERR
0x00	Mode ABZ	A	not(A)	B	not(B)	Z	not(Z)	ERR
0x0F	Mode 191/193	CPD	CPU	CP	nU/D	MR	nPL	ERR
0x01	Calibration 1	res.	res.	res.	IBN	PCH0	NCH0	res.
0x02	Calibration 2	PCH1	NCH1	PCH2	NCH2	VDC1	VDC2	res.
0x03	res. *	res.	res.	res.	res.	res.	res.	res.
0x04	res. *	res.	res.	res.	res.	res.	res.	res.
0x05	Test 5	PSIN	NSIN	PCOS	NCOS	res.	res.	res.
0x06	Test 6 (MUX=0x40)	X4	X6	X3	X5	X1	X2	res.
0x07	Calibration 3	VTs	VTth	res.	res.	VTTFE	VTTSE	ERR
0x08	res. *	res.						
0x09	res. *	res.						
0x0A	res. *	res.	res.	res.	res.	res.	res.	res.
0x0B	System Test	A_4	A_8	B_4	B_8	Z_{In}	TP1	ERR
0x0C	res. *	res.	res.	res.	res.	res.	res.	res.
0x0D	res. *	res.	res.	res.	res.	res.	res.	res.
0x0E	res. *	res.						
	Hints	*) Test function for iC-Haus device test only.						

Table 13: Operating Modes

Mode ABZ

In *Mode ABZ* A/B signals are generated and output via PA, NA, PB and NB. A configurable zero signal is provided at pins PZ and NZ. The differential RS422 line drivers are active; a Nx pin supplies a complementary signal which is the inversion of pin Px.

Mode 191/193

In *Mode 191/193* the output pins provide control signals for counter devices compatible with 74HC191 or 74HC193 according to the following table. The driving capability (SIK) and the slew rate (SSR) of the output drivers must be selected so that the clock pulses can be output with a short low pulse according to the chosen minimum phase distance (see Electrical Characteristics, 511).

Mode 191/193		
Pin	Signal	Description
PA	CPD	Clock Down Pulse
NA	CPU	Clock Up Pulse
PB	CP	Clock Pulse
NB	nU/D	Count Direction (0: up, 1: down)
PZ	MR	Asynch. Master Reset (active high) Signal is '1' if index position is reached, otherwise '0'.
NZ	nPL	Asynch. Parallel Load Input (active low) / Reset (active low) Signal is '0' if index position is reached, otherwise '1'.

Table 14: Operating mode for counter devices compatible with 74HC191 or 74HC193.

Calibration 1, 2, 3, Test 5
These modes are used to condition the input signals and calibrate iC-MQF. In mode *Calibration 1* the user can measure the IBN bias current and the zero channel analog signals are available (PCH0 and NCH0) (for zero channel calibration see page 25).

In mode *Test 5* the conditioned sine and cosine signals are output (PSIN, NSIN, PCOS and NCOS). In mode *Calibration 2* the conditioned sine and cosine signals are output with a gain which is reduced by factor 6 (PCH1, NCH1, PCH2 and NCH2). The intermediate potentials VDC1 and VDC2 are provided on Pin PZ and Pin NZ if VOS12 is set to 0x3. (For a description of the calibration process, see page 23).

In mode *Calibration 3* the internal temperature monitoring signals are provided. Calibration of the bias current source and temperature monitoring is described on page 17.

TEST 6
The input voltages at the pins X3 to X6 can be checked in mode *Test 6*. The following settings are required here:

- MUX = 0x40

System Test and Digital Calibration
This mode enables the signal conditioning to be adjusted using comparated sine and cosine signals. At a resolution of 8 the interpolator generates a switchpoint every 45 degrees. The objective of the calibration procedure is a pulse duty cycle of exactly 50% respectively for A_4, B_4 und A_8, B_8.

System Test		
Pin	Signal	Description
PA	A_4	Offset CH1
NA	A_8	Phase deviation from 90° between CH1 and CH2
PB	B_4	Offset CH2
NB	B_8	Amplitude deviation between CH1 and CH2
PZ	Z_{In}	Digital zero signal, unmasked
NZ	TP1	Verification of line count (pulses) between two zero pulses Low signal: verification running (state after power on reset) High signal: verification finished An error messaging at ERR is valid after the second zero signal (enable required).
The following settings are required for mode *System Test*: MODE = 0x0B, SELRES = 0x0002, SELHYS = 0xF, CFGABZ(7:4) = '0000'		

Table 15: Digital Calibration Signals

INPUT CONFIGURATION AND SIGNAL PATH MULTIPLEXER

All input stages are configured as instrumentation amplifiers and thus directly suitable for differential input signals. Referenced input signals can be processed; input X2 can be configured as a reference input. Both current and voltage signals can be processed, selected using R12 and R0.

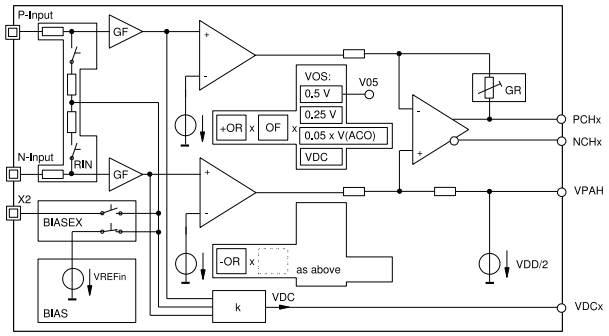


Figure 4: Signal conditioning input circuit.

Current Signals

In I Mode an input resistor Rin() becomes active at each input pin, converting the current signal into a voltage signal. Input resistance Rin() consists of a pad wiring resistor and resistor Rui() which is linked to the adjustable bias voltage source VREFin().

The table besides shows the possible selections, with Rin() giving the typical resulting input resistance (see Electrical Characteristics for tolerances). The input resistor should be set in such a way that intermediate potentials VDC1 and VDC2 lie between 125 mV and 250 mV (verifiable in mode *Calibration 2*).

NB. The input circuit is not suitable for back-to-back photodiodes.

Voltage Signals

In V mode an optional voltage divider can be selected which reduces unacceptably large input amplitudes to ca. 25 %. The circuitry is equivalent to the resistor chain in I mode; the pad wiring resistor is considerably larger here, however.

R12 **R0**	Addr 0x05, bit 3:0 Addr 0x04, bit 3:0		
Code	Nominal Rin()	Internal Rui()	I/V Mode
–000	1.7 kΩ	1.6 kΩ	current input
–010	2.5 kΩ	2.3 kΩ	current input
–100	3.5 kΩ	3.2 kΩ	current input
–110	4.9 kΩ	4.6 kΩ	current input
1—1	20 kΩ	5 kΩ	voltage input 4:1*
0—1	high impedance	1 MΩ	voltage input 1:1
Notes	When using X2 as reference input for single-ended signals use R12 = R0. *) VREFin is the voltage divider's footpoint. Input currents may be positive or negative (Vin > VREFin, or Vin < VREFin)		

Table 16: I/V Mode and Input Resistance

BIAS12 **BIAS0**	Addr 0x05, bit 6 Addr 0x04, bit 6
Code	Function
0	VREFin = 2.5 V for low-side current sinks (e.g. photodiodes with common anode at GNDS)
1	VREFin = 1.5 V for high-side currrent-sources (e.g. photodiodes with common cathode at VDDS) for voltage sources versus ground (e.g. iC-SM2, Wheatstone sensor bridges) for voltage sources with low-side reference (e.g. iC-LSHB, when using BIASEX = 11)
Notes	When using X2 as reference input for single-ended signals use BIAS12 = BIAS0.

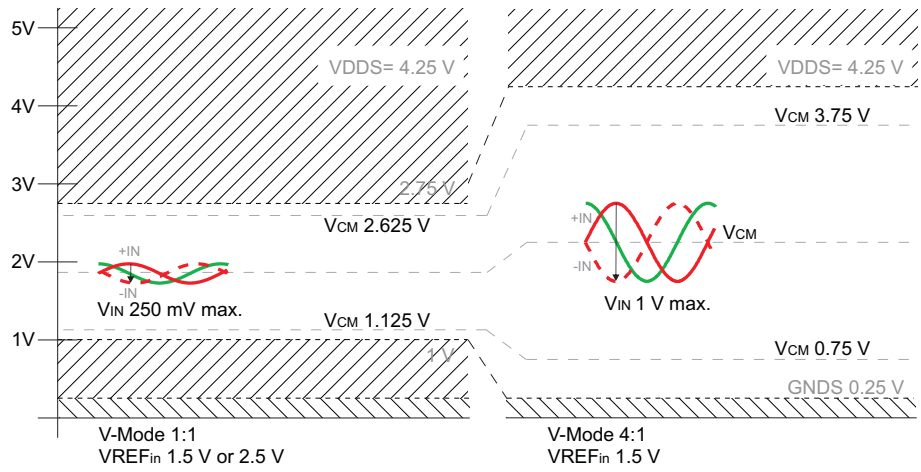
Table 17: Reference Voltage

Signal Path Multiplexer

The Pins X2 to X6 are assigned to the internal channels CH1 and CH2 according to Table 18, the signals for index channel CH0 are always connected to the pins X1 and X2.

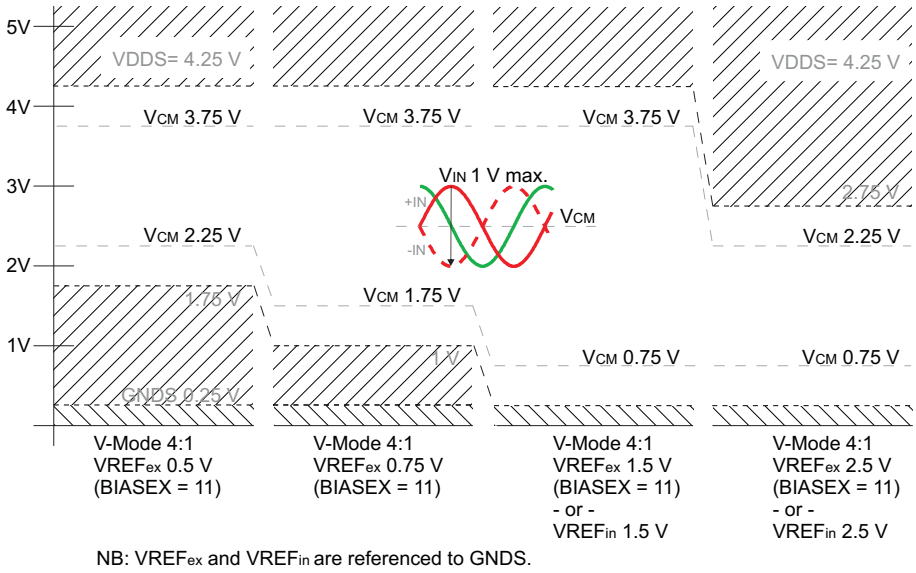
MUX(6:0)	Adr 0x03, bit 6:0						
Code	Function	PCH0i	NCH0i	PCH1i	NCH1i	PCH2i	NCH2i
MUX(2:0)	Adr 0x03, bit 2:0						
any	Fixed assignment	X1	X2	X4			
0	**Differential input** configuration				X6	X3	X5
2	Single crossing				X5	X3	X6
3	Double crossing				X3	X5	X6
4	**Single-ended** input configuration				X2	X3	X2
7	Single crossing				X2	X5	X2
MUX(3)	Adr 0x03, bit 3						
0	Default assignment	→ PCH0o	→ NCH0o				
1	Index signal inversion	→ NCH0o	→ PCH0o				
MUX(5:4)	Adr 0x03, bit 5:4						
0	Default assignment		X2				
2	X2 Output function: internal $VREF_{in}$ is output to X2		$VREF_{in}$ →X2				
3	X2 Reference function: external $VREF_{ex}$ supplies X2 and replaces internal VREFin		X2←$VREF_{ex}$				
MUX(6:0)	Adr 0x03, bit 6:0						
Code	Function	Pin PZ	Pin NZ	Pin PA	Pin NA	Pin PB	Pin NB
0x40	Default assignment TEST 6 (MODE = 0x6) OpAmp bypass function	X1	X2	PCH1o X4	NCH1o X6	PCH2o X3	NCH2o X5
Notes re. MUX(6:0)		Settings which are not explicitly specified may lead to an undesired chip function.					

Table 18: Input Multiplexer Function, Input Signal Mode, and Reference Selection



NB: $VREF_{in}$ is referenced to GNDS.

Figure 5: Permissible common mode range and maximum input signal for lowest gain (GR12 = 0x0, GF1, GF2 = 0x00); left side: voltage input 1:1, right side: voltage input 4:1.



NB: VREFex and VREFin are referenced to GNDS.

Figure 6: Permissible common mode range for voltage input 4:1 in dependancy to the reference voltage.

SIGNAL CONDITIONING CH1, CH2

It is recommended to use operating mode *Test 5* for the calibration of the sine signals. The sine signals are also available in operating mode *Calibration 2* for reasons of compatibility to iC-MQF, but the amplitudes are smaller (approx. 50% with respect to operating mode *Test 5*).

Alternatively, characteristic digital test signals are available for offset, amplitude and phase conditioning in operating mode *System Test*.

Gain Settings

The gain is set in four steps:

1. The sensor supply controller is shut down and the constant current source for the ACO output is set to a suitable output current (register ACOT = 0x2, ACOR and ACOS values close to the later operating point).

2. The coarse gain GR12 is selected so that differential signal amplitudes of ca. 6 Vpp are produced in operation mode *Test 5* (signal PSIN versus NSIN and PCOS versus NCOS).

3. Using fine gain factor GF2 the cosine signal amplitude is then adjusted to exactly 6 Vpp.

4. The sine signal amplitude can then be adjusted to the cosine signal amplitude via fine gain factor GF1.

This results in a total gain of GR12 * GFi for differential input signals.

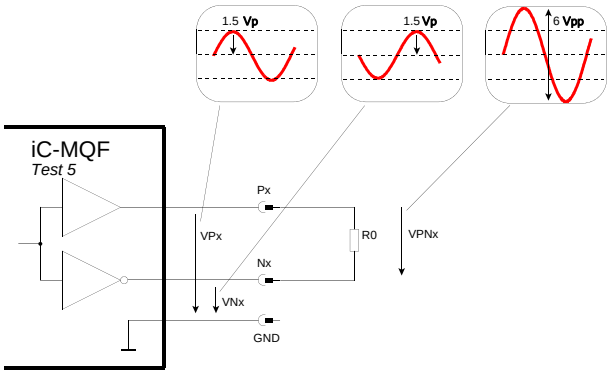


Figure 7: Definition of 6 Vpp signal. Termination R0 must be high-ohmic during all *Test* and *Calibration* modes.

GR12	Adr 0x0a, bit 2:0	
Code	Range R12=0x9	Range R12≠0x9
0x0	3.0	12.0
0x1	6.0	24.6
0x2	7.8	31.8
0x3	10.2	40.2
0x4	13.2	52.2
0x5	15.6	63.0
0x6	19.8	79.2
0x7	24.0	96.0
Notes	Valid for all operation modes except for *Calibration 2* (reduces gain to 1/6).	

Table 19: Gain Range CH1, CH2 (coarse)

GF2	Adr 0x0c, bit 4:0
Code	Factor
0x00	1.00
0x01	1.06
...	$6.25\,\frac{GF2}{31}$
0x1F	6.25

Table 20: Fine Gain Factor CH2

GF1	Adr 0x0b, bit 6:0, Adr 0x0a, bit 7:4
Code	Factor
0x000	1.0
0x001	1.0009
...	$6.25\,\frac{GF1}{1984}$
0x7FF	6.6245

Table 21: Fine Gain Factor CH1

Offset Calibration CH1, CH2

In order to calibrate the offset the reference source must first be selected using VOS12. Two fixed voltages and two dependent sources are available for this purpose. The fixed voltage sources should be selected for external sensors which provide stable, self-regulating signals.

So that photosensors can be operated in optical encoders iC-MQF tracks changes in offset voltages via the signal-dependent source VDC when used in conjunction with the controlled sensor current source for LED supply (pin ACO). The VDC potential automatically tracks higher DC photocurrents. To this end intermediate potentials VDC1 and VDC2 must be adjusted to a minimal AC ripple using the selectable k factor (this calibration must be repeated when the gain setting is altered).

The feedback of pin voltage V(ACO) fulfills the same task as source VDC when MR bridge sensors are supplied by the controlled sensor current source or by supply VDDS.

VOS12	Addr 0x05, bit 5:4
Code	Type of source
0x0	Feedback of ACO pin voltage: V(ACO)/20 for supply-dependent differential voltage signals for Wheatstone sensor bridges to measure VDDS
0x1, 0x2	Fixed reference: V05 of 500 mV, V025 of 250 mV for single-ended current or voltage signals for single-ended or differential stabilized signals (regulated sensor or waveform generator)
0x3	Self-tracking sources VDC1, VDC2 (125...250 mV) for differential current signals for differential voltage signals*
Notes	*) Requires MUX(5:4) = 3 and the sensor's reference connected to input X2; refer to Elec. Char. No. 105 for acceptable input voltage).

Table 22: Offset Reference Source CH1, CH2

VDC1 **VDC2**	Addr 0x0E, bit 1:0; Addr 0x0D, bit 7:0 Addr 0x0F, bit 5:0; Addr 0x0E, bit 7:4
Code	$VDCi = (1 - k) \cdot VPi + k \cdot VNi$
0x000	$k = 1/3$
0x001	$k = 0.3386$
...	$k = 1/3 + 1/3 \cdot Code/1023$
0x200	$k = 0.5000$ (center setting)
...	...
0x3FF	$k = 2/3$
Notes	Adjustment is required only if VOS12 = 0x3

Table 23: Intermediate Voltages CH1, CH2

The offset calibration range for CH1 and CH2 is set using OR1 and OR2. Both sine and cosine signals are then calibrated using factors OF1 and OF2. The calibration target is reached when the DC fraction of the differential signals PCHi versus NCHi is zero.

OR1 **OR2**	Addr 0x10, bit 1:0 Addr 0x10, bit 3:2
Code	Range
0x0	x1
0x1	x2
0x2	x6
0x3	x12

Table 24: Offset Range CH1, CH2

OF1 **OF2**	Addr 0x11, bit 6:0; Addr 0x10, bit 7:4 Addr 0x13, bit 2:0; Addr 0x12, bit 7:0		
Code	Factor	Code	Factor
0x000	0	0x400	0
0x001	0.00098	0x401	– 0.00098
...	+ Code / 1023	...	– (Code - 1024) / 1023
0x3FF	1	0x7FF	– 1

Table 25: Offset Factors CH1, CH2

Phase Correction CH1 vs. CH2

The phase shift between CH1 and CH2 can be adjusted using parameter PH12. Following phase calibration other calibration parameters may have to be readjusted (those as amplitude compensation, intermediate potentials and offset voltages).

PH12	Addr 0x14, bit 5:0; Addr 0x13, bit 7:4		
Code	Correction angle	Code	Correction angle
0x000	0 °	0x200	0 °
0x001	+ 0.0204 °	0x201	– 0.0204 °
...	+ 10.42 ° · PH12 /511	...	– 10.42 ° · (PH12 - 512) /511
0x1FF	+ 10.42 °	0x3FF	– 10.42 °

Table 26: Phase Correction CH1 vs. CH2

SIGNAL CONDITIONING CH0

The voltage signals needed to calibrate the zero channel are available in mode *Calibration 1*. The relative phase position of the ungated zero signal Zin compared to A and B can be determined in mode *System Test*.

Gain Settings CH0

The CH0 gain is set in the following steps:

1. The sensor supply controller is shut down and the constant current source for the ACO output is set to the same values as during the calibration of CH1 and CH2 (registers ACOT, ACOR and ACOS).

2. The coarse gain is selected so that a differential signal amplitude of ca. 1 Vpp is produced internally (signal PCH0 versus NCH0).

3. GF0 then permits fine gain adjustment to 1 Vpp. The total gain is accrued from GR0 x GF0.

GR0	Addr 0x07, bit 6:4	
Code	Range R0 = 0x9	Range R0 ≠ 0x9
0x0	0.5	2.0
0x1	1.0	4.1
0x2	1.3	5.3
0x3	1.7	6.7
0x4	2.2	8.7
0x5	2.6	10.5
0x6	3.3	13.2
0x7	4.0	16.0

Table 27: Gain Range CH0

GF0	Addr 0x08, bit 4:0
Code	Factor
0x00	1.00
0x01	1.06
...	$6.25^{\frac{GF0}{31}}$
0x1F	6.25

Table 28: Fine Gain Factor CH0

Offset Calibration CH0

The offset reference source is selected with VOS0. The offset compensation is set with OR0 and OF0 (see Offset Calibration CH1 and CH2 for further information).

VOS0	Addr 0x04, bit 5:4
Code	Source
0x0	0.05 · V(ACO)
0x1	0.5 V
0x2	0.25 V
0x3	VDC1

Table 29: Offset Reference Source CH0

OR0	Addr 0x07, bit 1:0
Code	Range
0x0	x1
0x1	x2
0x2	x6
0x3	x12

Table 30: Offset Range CH0 (coarse)

OF0	Addr 0x09, bit 5:0		
Code	Factor	Code	Factor
0x00	0	0x20	0
0x01	0.0322	0x21	– 0.0322
...	+ Code /31	...	– (Code - 32) /31
0x1F	1	0x3F	– 1

Table 31: Offset Factor CH0 (fine)

SIGNAL LEVEL CONTROL and SIGNAL MONITORING

iC-MQF's signal level controller can keep the input signals for the sine-to-digital converter constant, regardless of temperature and aging effects, when using control output ACO for tracking the sensor supply.

ACOR(1:0) presets the output current range of pin ACO, the control's highside current source output, and ACOT(1:0) defines its control mode.

The resulting internal signal amplitude and the control's operating range are both monitored and thus can be used for error messaging.

ACOR (1:0)	Addr 0x15, bit 7:6
Code	Function
00	5 mA - Range
01	10 mA - Range
10	25 mA - Range
11	50 mA - Range

Table 32: ACO Output Current Range (applies for control modes and constant current source)

ACOT (1:0)	Addr 0x16, bit 1:0
Code	Function
00	Sine/cosine square control
01	Sum control
10	Constant current source
11	Not permitted (device test only)

Table 33: ACO Output Control Mode

Notice: Excessive input signals or internal signal clipping can interfere control operation, so that the preset operating point may not be reached (upon power up) or maintained (upon disturbances). Use Control Error 2 and Signal Error 1 for monitoring and configure EMASKA accordingly.

The standard control mode is *square control* which uses (sine^2 + cosine^2) to adjust the ACO output current. ACOS(4:0) determines the internal signal amplitudes within the closed-loop control and, simultaneously, the amplitude monitoring thresholds. The ideal setpoint here is 3 Vpp referred to the sin/cos test signals available in operating mode *Test 5*.

With *sum control* mode selected, the DC references (VDC1 + VDC2) are used to adjust the output current of pin ACO.

The *constant current source* is intended for signal conditioning purposes, i.e. for the adjustment of gain, offset and phase correction values without interference by signal level controlling.

ACOS (4:0)	Addr 0x15, bit 5:1	
Code	**Square control** ACOT = 00	
0x00	Vpp() ≈ 1800 mV (60 %)	
0x01	Vpp() ≈ 1830 mV (61 %)	
...	...	$\approx 1800\,mV\,\frac{77}{77-(1.25*Code)}$
0x19	Vpp() ≈ 3000 mV (98 %)	
...	...	
0x1F	Vpp() ≈ 3600 mV (120 %)	

Table 34: Square Control Setpoint (internal sin/cos signal amplitude)

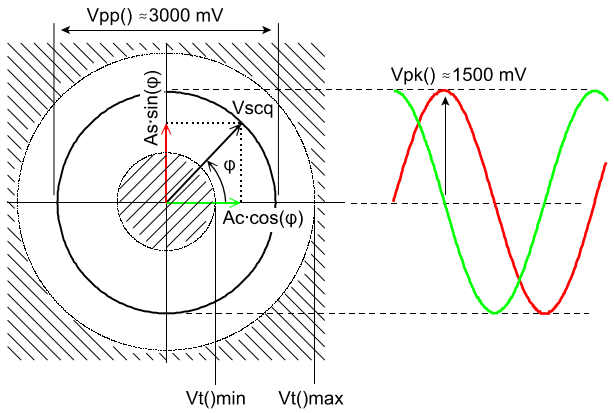


Figure 8: Signal monitoring and test signals in *Test 5* mode (example for ACOS(4:0) = 0x19).

Signal monitoring and limits			
ADJ (4:0)	Vt()min ... max	ADJ (4:0)	Vt()min ... max
0x00	0.72 V...2.34 V	0x19	1.2 V ...3.9 V
0x01	0.732 V...2.38 V	...	...
...	...	0x1F	1.44 V...4.68 V
Notes	All values nominal, see also Elec. Char. Nos. 605, 606		

Table 35: Signal Monitoring

The signal monitoring thresholds are tracked according to ACOS (4:0) and fit for *square control mode*. When using *sum control mode* a different operating point can be required for which the monitoring thresholds may not be suitable. In this case signal monitoring should be disabled via the error mask (see EMASKA etc.).

ACOS (4:0)	Addr 0x15, bit 5:1
Code	**Sum control** ACOT = 01
0x00	VDC1 + VDC2 ≈ 245 mV
0x01	VDC1 + VDC2 ≈ 249 mV
...	... $\approx 245mV\frac{77}{77-(1.25*Code)}$
0x1F	VDC1 + VDC2 ≈ 490 mV

Table 36: Sum Control Setpoint (DC average)

ACOS (4:0)	Addr 0x15, bit 5:1
Code	**Constant current source** ACOT = 10
0x00	I(ACO) ≈ 3.125% Isc(ACO)
0x01	I(ACO) ≈ 6.25% Isc(ACO)
...	... $\approx 3.125\% * (Code + 1) * Isc(ACO)$
0x1F	I(ACO) ≈ 100% Isc(ACO)
Notes	See Elec. Char. No. 602 for Isc(ACO)

Table 37: Current Source Setpoint (ACO output current)

SINE-TO-DIGITAL CONVERSION

SELRES	Addr 0x21, bit 6:0; Addr 0x20, bit 7:0		
Value	STEP Angle Steps Per Period	IPF Interpolation Factor	fin()max Permissible Input Frequency (@ MTD)
0x0001	4	1	200 kHz (0x1)
0x0002	8	2	200 kHz (0x1)
0x0004	16	4	200 kHz (0x1)
0x0005	20	5	200 kHz (0x1)
0x0008	32	8	200 kHz (0x1)
0x000A	40	10	200 kHz (0x1)
0x0014	80	20	166 kHz (0x1)
0x0019	100	25	133 kHz (0x1)
0x0028	160	40	83 kHz (0x1)
0x0032	200	50	66 kHz (0x1)
0x0064	400	100	20 kHz (0x4*)
0x007D	500	125	16 kHz (0x4*)
0x00C8	800	200	7.1 kHz (0x6*)
0x00FA	1000	250	5.7 kHz (0x6*)
0x01F4	2000	500	2.5 kHz (0x7*)
0x03E8	4000	1000	0.8 kHz (0x8*)
Notes	Other settings are not allowed. *) Recommended MTD setting, refer to Design Review page 36.		

Table 38: Converter Resolution

iC-MQF's converter resolution is selected with SELRES. For a resolution of 4, four angle steps per input signal period are generated so that the switching frequency at the A and B output matches the sine frequency at the input.

The programmable converter hysteresis is determined by SELHYS. It is set in multiples of the increment size and may have a maximum of 45° of the input signal period.

SELHYS	Addr 0x1F, bit 3:0		
Code	Function	Code	Function
0x0	nearly none	0x8	2.0°
0x1	0.09°	0x9	4.0°
0x2	0.18°	0xA	6.0°
0x3	0.36°	0xB	8.0°
0x4	0.45°	0xC	10.0°
0x5	0.72°	0xD	11.25°
0x6	1.0°	0xE	22.5°
0x7	1.5°	0xF	45°

Table 39: Converter Hysteresis

OUTPUT SETTINGS AND ZERO SIGNAL

The interpolation factor IPF determines the number of A/B signal cycles per input signal period. These A/B signal cycles are counted in the internal register POS, which can be used to blank the zero pulse.

POS is set to 0 if the input sine/cosine phase angle is zero degrees, its maximum value is POS_{max} = IPF-1. The internal A/B signal cycle adheres to the following pattern:

A	1	1	0	0
B	1	0	0	1

Table 40: Internal A/B Signal Cycle

Inversions and reversals can be selected for the output of the A/B/Z signals and the zero signal can be blanked with any combination of the internal A and B signal by programming parameter CFGABZ.

CFGABZ	Addr 0x1D, bit 7:0
Bit	Function and Description
7	Output inversion for channel A: PA<>NA PA = P1i xor CFGABZ(7)
6	Output inversion for channel B: PB<>NB PB = P2i xor CFGABZ(6)
5	Output inversion for index channel: PZ<>NZ PZ = P0i xor CFGABZ(5)
4	Exchange of the A/B signals 0: P1i = A, P2i = B 1: P1i = B, P2i = A
	Zero Signal Blanking CFGABZ(3:0)
3	Enable for A = 1, B = 1
2	Enable for A = 1, B = 0
1	Enable for A = 0, B = 0
0	Enable for A = 0, B = 1

Table 41: Output Logic

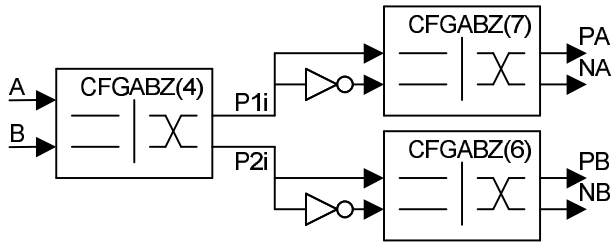


Figure 9: Signal Path from A and B to PA/NA and PB/NB

Zero Signal Generation

The generation of the zero signal is dependant on the internal signal Z_{In} which is produced by comparing the calibrated CH0 input signals. The offset calibration of CH0 influences the width of the Z_{In} signal. The correct position of Z_{In} should be checked before configuring the zero signal blanking logic. This is possible by comparing the Z_{In} signal with the PA/PB signals in *Mode ABZ*: Z_{In} is displayed on pin ERR if EMASKA = 0x010 and EMTD = 0x0 is programmed.

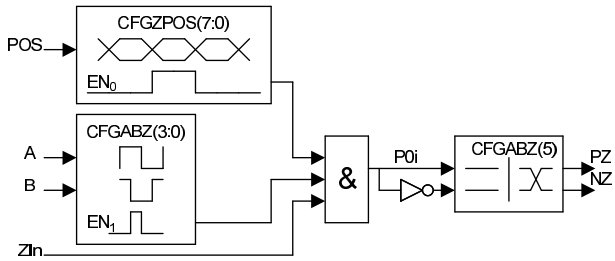


Figure 10: Signal path from Z_{In} to PZ/NZ

The blanking of the Z_{In} signal by CFGZPOS is relative to the internal A/B cycle count POS. Multiple settings of CFGZPOS are possible at high resolutions, choose a setting which centers the output signal PZ in relation to Z_{In}. Attention: Programming CFGZPOS to a cycle count larger than POS_{max} leads to undetermined zero signal prevention.

CFGZPOS	Addr 0x1E, bit 7:0
Bit	Description
7	0: Mask not used 1: Mask Enable (zero signal blanking with POS enabled)
(6:0)	For IPF < 200: blanking of Z_{In} if POS ≠ CFGZPOS(6:0) For IPF ≥ 200: blanking of Z_{In} if POS ≠ 8 * CFGZPOS(6:0)
Example	Assuming an index window where sine crosses cosine (45 °): CFGZPOS = 13 for IPF 100, respectively CFGZPOS = 16 for IPF 1000

Table 42: Zero Signal Positioning

ENZFF	Addr 0x02, bit 4
Code	Description
0	Zero signal output with state change of P0i
1	Zero signal output synchronized with A/B signal
Note	This function requires an index gating window Z_{in} that fully overlaps the selected AB cycle for indexing.

Table 43: Zero Signal Synchronization

Output Driver Configuration

The output drivers can be used as push-pull, lowside or highside drivers; the mode of operation is determined by TRIHL(1:0).

The slew rate can be set using SSR to suit the length of the cable. Lower slew rates are used to avoid steep edges when transmitting via short wires, but can result in a limiting of the maximum permissible output frequency. (For example, this frequency is 300 kHz at a slew rate of 300 ns if the RS422 specification is to be adhered to. (the tolerances in Electrical Characteristics, numbers 506/507, must be observed)).

The short-circuit current can be set by SIK and can be minimized when connecting to on board logic or to an external 24 V line driver. If the outputs are used as RS422-compatible 5 V drivers, it is recommended that SIK = 11 to keep the power dissipation of iC-MQF low.

TRIHL	Addr 0x22, bit 1:0
Code	Function
00	Push-pull operation
01	Highside driver mode (P channel open drain)
10	Lowside driver mode (N channel open drain)
11	Not permitted

Table 44: Output Drive Mode

SSR	Addr 0x22, bit 3:2
Code	Function
00	Nominal value 12 ns
01	Nominal value 25 ns
10	Nominal value 80 ns
11	Nominal value 220 ns
Note	See Elec. Char. 505/ 506

Table 45: Output Slew Rate

SIK	Addr 0x22, bit 5:4
Code	Function
00	typ. 2 mA, linking logic or driver ICs
01	typ. 8 mA
10	typ. 40 mA
11	typ. 100 mA, recommended for RS422
Note	See Elec. Char. 503/ 504

Table 46: Output Short-Circuit Current

Minimum Transition Distance

Register CFGOSZ(2:0) calibrates the timing of t_{MTD}, the minimum transition distance in *Mode ABZ*, and tclk()lo, the low pulse duration of the clock signals in *Mode 191/193* (see Elec.Char., no. 511 and no. 514).

CFGOSZ	Addr 0x25, bit 2:0		
Code k		Code k	
0x0	140 %	0x4	105 %
0x1	130 %	0x5	100 %
0x2	120 %	0x6	92 %
0x3	110 %	0x7	n/a

Table 47: Calibration of MTD Oscillator

The calibration must be executed in *Mode 191/193* with register MTD(3:0) = 0x0F. Apply a sine signal at the inputs X3 to X6 and observe the length of the low pulses at pin PB. The setting of CFGOSZ is correct if the observed tclk()lo is close to the nominal value of Elec. Char. no. 511.

MTD	Addr 0x1F, bit 7:4	
Code	*Mode ABZ*: t_{MTD}	*Mode 191/193: tclk()lo*
0x0	not available	not available
0x1	50 ns	not available
0x2	75 ns	not available
0x3	100 ns	50 ns
0x4	125 ns	62.5 ns
0x5	150 ns	75 ns
0x6	175 ns	87.5 ns
0x7	200 ns	100 ns
0x8	300 ns	150 ns
0x9	400 ns	200 ns
0xA	600 ns	300 ns
0xB	800 ns	400 ns
0xC	1.0 µs	500 ns
0xD	1.2 µs	600 ns
0xE	1.4 µs	700 ns
0xF	1.6 µs	800 ns
Note	All timing specifications are nominal values, see Elec. Char. 514 for tolerances.	

Table 48: Minimum Transition Distance

If CFGOSZ(2:0) is set correctly, the minimum transition distance of the output signals can be preset by MTD(3:0). This setting limits the maximum possible output frequency to ensure a safe transmission to counters, which permit only a low input frequency and thus cannot debounce spikes. The configuration of the RS422 output drivers (with regard to the driver current and slew rate) and the cable length must be taken into account when choosing the minimum edge distance.

Signal Filter

ENF	Addr 0x03, bit 7
Code	Function
0	Disabled
1	Noise limiting signal filter enabled (default)

Table 49: Noise Filter

ERROR MONITORING AND ALARM OUTPUT

iC-MQF monitors the input signals, the internal interpolator and the sensor supply controller via which the input signal levels are stabilized. If the sensor supply tracking unit reaches its control limits this can be interpreted as an end-of-life message, for example.

Three separate error masks stipulate whether error events are signaled as an alarm via I/O pin ERR (mask EMASKA), whether they cause the RS422 line drivers to shutdown or not (mask EMASKO) or whether they are stored in the EEPROM (mask EMASKE).

Alarm Output: I/O-pin ERR

Pin ERR is operated by a current-limited open-drain output driver and has an internal pull-up which can be disabled. The ERR pin also acts as an input for external system error messaging and for switching iC-MQF to test mode for which a voltage of larger than VTMon must be applied (see page 33). Interpretation of an external system error message and the phase of the message output is configured by EPH, the minimum indication time by EMTD.

EPH	Addr 0x1A, bit 4	
Code	State on error	State w/o error
0*	active low	high impedance, with input function for a low-active system error;
1	high impedance	active low
Notes	*) Pin ERR is disabled during driver shutdown and cannot indicate errors in this case.	

Table 50: I/O Logic, Alarm Output ERR

EMTD	Addr 0x18, bit 6:4		
Code	Indication Time	Code	Indication Time
0x0	0 ms	0x4	50 ms
0x1	12.5 ms	0x5	62.5 ms
0x2	25 ms	0x6	75 ms
0x3	37.5 ms	0x7	87.5 ms

Table 51: Min. Indication Time, Alarm Output ERR

EPU	Addr 0x1A, bit 5
Code	Function
0	No internal pull-up
1	Internal 300 µA pull-up current source active

Table 52: Pull-Up Enable, Alarm Output ERR

EMASKA	Addr 0x18, bit 1:0; Addr 0x17, bit 7:0
Bit	Error event
9	Line count error (wrong count of sine periods between two zero pulses)
8	Temporal tracking error (out-of-sync: position output differs from actual angle, e.g. after cycling power)
7	Loss of tracking (excessive input frequency)
6 *	Configuration error (SDA or SCL pin error, no acknowledge signal from EEPROM or invalid check sum)
5	Excessive temperature warning
4	Ungated index enable signal Z_{In} (comparated X1/X2 inputs for CFGABZ and CFGZPOS adjustment, at EMTD = 0x0)
3	Control error 2: range at max. limit
2	Control error 1: range at min. limit
1	Signal error 2: clipping
0	Signal error 1: loss of signal (poor differential amplitude**, wrong s/c phase)
Code	Function
1	Enable: event changes state of pin ERR (if EMASKO does not disable the output function).
0	Disable: event does not affect pin ERR.
Notes	*) Pin ERR can not pull low on configuration error, use high-active error logic instead (EPH = 1); **) Also due to excessive input signals or internal signal clipping.

Table 53: Error Mask Alarm Output ERR

Line Count Error

Line count monitoring is particularly interesting for encoder systems. iC-MQF counts the number of sine cycles between two adjacent zero pulses and compares it to the reference value LINECNT. In case of a deviation the line count error is set. The check is paused if the direction of rotation changes, and is restarted on the next zero pulse. During mode *System Test* signal TP1 indicates when a first line count check has finished.

LINECNT	Addr 0x24, bit 5:0; Addr 0x23, bit 7:0	
Code	Function Value	Line Count (CPR)
0x0000	0	1
...	...	Code + 1
0x3FFF	16383	16384
Example	Code disc of 256 CPR → LINECNT = 255	

Table 54: Line Count Reference

Excessive Temperature Warning

Exceeding the temperature warning threshold T_w (corresponds to T_2, refer to Temperature Sensor, page 17) can be signaled at pin ERR or used to shut down the line drivers (via mask EMASKO). The temperature

warning is cleared if the temperature falls below T_w -T_{hys}.

Notice: If the temperature shutdown threshold T_{off} = T_w + ΔT is exceeded, the line drivers are shut down independently of EMASKO. For ΔT refer to Elec. Char. E07.

Driver Shutdown

Driver shutdown is a precaution to protect iC-MQF. Pin ACO is set to the 5mA range, the line drivers and pin ERR are tristate during driver shutdown.

Driver shutdown due to overheating or due to a configuration error is always enabled. Configuration errors are SDA or SCL pin error, no acknowledge signal from EEPROM or invalid checksum. EMASKO is used program driver shutdown due to other error events.

PDMODE	Addr 0x1A, bit 6
Code	Function
0	Driver shutdown terminates with the error event
1	Permanent driver shutdown until cycling power

Table 55: Driver Activation

EMASKO	Addr 0x1A, bit 1:0; Addr 0x19, bit 7:0
Bit	Error event
9	Line count error (wrong count of sine periods between two zero pulses)
8	Temporal tracking error (out-of-sync: position output differs from actual angle, e.g. after cycling power)
7 *	Loss of tracking (excessive input frequency)
6 **	—
5	Excessive temperature warning
4	System error: I/O pin ERR pulled to low by an external error signal (only permitted with EPH = 0)
3	Control error 2: range at max. limit
2	Control error 1: range at min. limit
1	Signal error 2: clipping
0	Signal error 1: loss of signal (poor differential amplitude***, wrong s/c phase)
Code	Function
1	Enable: event causes a driver shutdown
0	Disable: output drivers remain active
Notes	*) Program EMASKO(7) = 0 to EEPROM. **) Program EMASKO(6) = 0 to EEPROM. This allows to reenable the drivers after a configuration error by toggling bit END (set zero, then one). If set 1, the driver shutdown persists and can not be resolved. ***) Also due to excessive input signals or internal signal clipping.

Table 56: Error Mask Driver Shutdown

Error Logging

Error information can be stored in the EEPROM. Only errors enabled by EMASKE are logged. The first error in the lifetime of the product is stored in ERR1. The last occurred error is stored in ERR2.

The EEPROM has an additional memory area in which all errors are accumulated (ERR3). Only errors enabled by EMASKE are logged and only the fact that this error has occurred is logged, with no information as to the time and count of appearance of that error given. Error logging can be used to statistically evaluate the causes of system failure, for example.

iC-MQF enters standby and the line drivers are shut down if an I^2C communication error occurred during a write access to the EEPROM. (iC-MQF can be reenabled with bit END if EMASKO(6) is zero.)

Clearing ERR1, ERR2 and ERR3

The error information in the EEPROM can be cleared during standby: First, set END to zero, then clear the errors in the EEPROM (Dev-ID 0x50, Addr. 0x30-0x33) *and* in the corresponding registers of iC-MQF (Dev-ID 0x55, Addr. 0x30-0x33). Finally, iC-MQF can be enabled by setting END to one.

EMASKE	Addr 0x1C, bit 1:0; Addr 0x1B, bit 7:0
Bit	Error event
9	Line count error
8 *	—
7 *	—
6 *	—
5	Excessive temperature warning
4	System error
3	Control error 2
2	Control error 1
1	Signal error 2
0	Signal error 1
Code	Function
1	Enable: event is logged
0	Disable: event is not logged
Note	*) Mandatory programming is zero.

Table 57: Error Mask EEPROM Savings

ERR1	Addr 0x31, bit 1:0; Addr 0x30, bit 7:0
ERR2	Addr 0x32, bit 3:0; Addr 0x31, bit 7:2
ERR3	Addr 0x33, bit 5:0; Addr 0x32, bit 7:4
Bit	Error Event
9:0	Assignation according to EMASKE
Code	Function
0	No event
1	Logged error event

Table 58: Error Protocol

REVERSE POLARITY PROTECTION

iC-MQF is protected against a reversal of the supply voltage and has short-circuit-proof, error-tolerant line drivers. A defective device cable or one wrongly connected is tolerated by iC-MQF. All circuitry components which draw the monitored supply voltage from VDDS and GNDS are also protected.

The following pins are also reverse polarity protected: PA, NA, PB, NB, PZ, NZ, ERR, VDD, GND and ACO.

Conditions: This is based on the condition that GNDS only receives load currents from VDDS. The maximum voltage difference between GNDS and another pin should not exceed 6 V, the exception here being pin ERR (see *Test Mode* page 33).

TEST MODE

iC-MQF switches to test mode if a voltage larger than VTMon is applied to pin ERR (precondition: EMODE(0) = 1). In response iC-MQF transmits its configuration settings as current-modulated data using I/O pin ERR either directly from the RAM (for EMODE(2) = 1) or after re-reading the EEPROM (for EMODE(2) = 0). If the voltage at pin ERR falls below VTMoff, test mode is terminated and data transmission aborted.

The clock rate for the data output is determined by ENFAST. Two clock rates can be selected: 780 ns for ENFAST = 1 or 3.125 µs for ENFAST = 0 (see Electrical Characteristics, B12, for clock frequency and tolerances).

Data is output in Manchester code via two clock pulses per bit. To this end the lowside current source switches between a Z state (OFF = 0 mA) and an L state (ON = 2 mA).

The bit information lies in the direction of the current source switch:
Zero bit: change of state Z → L (OFF to ON)
One bit: Change of state L → Z (ON to OFF)

Transmission consists of a start bit (a one bit), 8 data bits and a pause interval in Z state (the timing is identical with an EEPROM access via the I^2C interface).

Example: byte value = 1000 1010
Transmission including the start bit: 1 1000 1010
In Manchester code: LZ LZZL ZLZL LZZL LZZL

Decoding of the data stream:

ZZZZZZ LZ LZ ZL ZL ZL LZ ZL LZ ZL ZZZZZZ
Pause 1 1 0 0 0 1 0 1 0 Pause

EMODE	Addr 0x1C, bit 6:4	
Code 2:0	Function during test mode	Function following test mode
000	Normal operation	Normal operation
010	Normal operation	Repeated read out of EEPROM
001	Transmission of error and EEPROM OEM data (address range 0x24 to 0x7F)	Repeated read out of EEPROM
011	Transmission of EEPROM contents (0x0-0x7F)	Repeated read out of EEPROM
101	Transmission of error and RAM OEM data (ENSL = 1, address range 0x3B to 0x43)	Repeated read out of EEPROM
111	Transmission of RAM contents (0x0-0x7F) (ENSL = 1)	Repeated read out of EEPROM
100	Not allowed	
110	Not allowed	

Table 59: Test Mode

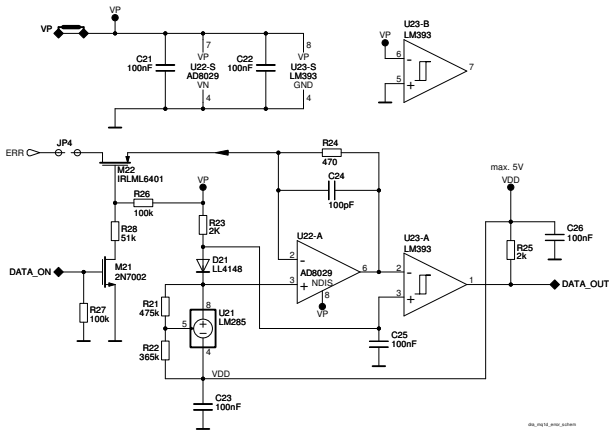


Figure 11: Example circuit for the decoding and conversion of the current-modulated signals to logic levels.

Quick programming in the single master system

For the purpose of signal conditioning it is possible to reprogram iC-MQF quickly. If test mode is quit and EMODE(1:0) ≠ 00, iC-MQF reads the configuration data in again.

In operating modes *Mode ABZ*, *System Test* and *Mode 191/193* the content of the EEPROM is read in its entirety. For other modes the address area is limited to 0x0-0x31 so that the configuration time for either calibration or IC testing is shortened.

If the setup is switched to test mode during the readin procedure, readin is aborted and only repeated once test mode has been terminated.

Quick programming in the multimaster system

Fast programming of iC-MQF, byte for byte, is possible with a multimaster-competent programming device. To this end the integrated I^2C slave mode must be enabled by ENSL; iC-MQF then reacts to the device ID 0x55.

If no EEPROM is connected, iC-MQF automatically sets the I^2C slave mode enable (after a maximum of 150 ms, see Electrical Characteristics, D11) and deactivates the digital section (ENSL = 1 and END = 0 are set). Any number of bytes can be written at any one time; the received data is accepted directly into the RAM register. After programming END = 1 must be set to restart sine-to-digital conversion in the selected mode of operation.

GENERAL APPLICATION HINTS

Refer to the datasheet of iC-MQ.

APPLICATION NOTES: SIGNAL CONDITIONING

Regarding a description of the principle signal conditioning procedure refer to the datasheet of iC-MQ.

Signal Conditioning Example 1:

Photodiode array connected to current inputs, LED supply with constant current source

Step	Operating Mode	Calibration and Signal
1.		Presets VOS12= 0x3, GF1= 0x400, VDC1= 0x200, OF1= 0x0, GF2= 0x10, VDC2= 0x200, OF2= 0x0 Example: LED current approx. 6.25 mA ACOT(1:0)= 0x2 (constant current source), ACOR(1:0)= 0x3 (range 50 mA), ACOS(4:0)= 0x04 (value 12.5)
2.		Calibration of Channel 1:
	Test 5	Parameter GR12: Adjust the diff. signal at PA vs. NA to approx. 6 Vpp amplitude
	Test 5	Parameter GF1: Adjust the diff. signal at PA vs. NA to exactly 6 Vpp amplitude
	Calibration 2	Parameter VDC1: Minimize the AC fraction of VDC1 at PZ (ripple < 10 mVpeak)
	Test 5	Parameter OR1, OF1: Minimize the DC fraction of the diff. signal PA vs. NA (< 5 mVdc)
3.	*Test 5*	Calibration of Channel 2:
	Test 5	Parameter GF2: Adjust the diff. signal at PB vs. NB to exactly 6 Vpp amplitude
	Calibration 2	Parameter VDC2: Minimize the AC fraction of VDC2 at NZ (ripple < 10 mVpeak)
	Test 5	Parameter OR2, OF2: Minimize the DC fraction of the diff. signal PB vs. NB (< 5 mVdc)
4.	*System Test*	1. Iteration, Calibration of Channel 1 vs. Channel 2: Parameter OF1: Adjust duty ratio of A_4 at PA to 50 % Parameter OF2: Adjust duty ratio of B_4 at PB to 50 % Parameter PH12: Adjust duty ratio of A_8 at NA to 50 % Parameter GF1: Adjust duty ratio of B_8 at NB to 50 %
5.	*Calibration 2*	Repeated Adjustment of Intermediate Voltages, VDC1 and VDC2: Parameter VDC1: Minimize the AC fraction of VDC1 at PZ Parameter VDC2: Minimize the AC fraction of VDC2 at NZ
6.	*System Test*	2. Iteration, Calibration of Channel 1 vs. Channel 2: Parameter OF1: Adjust duty ratio of A_4 at PA to 50 % Parameter OF2: Adjust duty ratio of B_4 at PB to 50 % Parameter PH12: Adjust duty ratio of A_8 at NA to 50 % Parameter GF1: Adjust duty ratio of B_8 at NB to 50 %

Table 60: Conditioning example 1

Signal Conditioning Example 2:

Encoder supplying 100 mVpp to voltage inputs

Step	Operating Mode	Calibration and Signal
1.		Presets VOS12= 0x1, GF1= 0x400, OF1= 0x0, GF2= 0x10, OF2= 0x0
2.		Calibration of Channel 1:
	Test 5	Parameter GR12: Adjust the diff. signal at PA vs. NA to approx. 6 Vpp amplitude
	Test 5	Parameter GF1: Adjust the diff. signal at PA vs. NA to exactly 6 Vpp amplitude
	Test 5	Parameter OR1, OF1: Minimize the DC fraction of the diff. signal PA vs. NA (< 5 mVdc)
3.	*Test 5*	Calibration of Channel 2:
	Test 5	Parameter GF2: Adjust the diff. signal at PB vs. NB to exactly 6 Vpp amplitude
	Test 5	Parameter OR2, OF2: Minimize the DC fraction of the diff. signal PB vs. NB (< 5 mVdc)
4.	*System Test*	Calibration of Channel 1 vs. Channel 2: Parameter OF1: Adjust duty ratio of A_4 at PA to 50 % Parameter OF2: Adjust duty ratio of B_4 at PB to 50 % Parameter PH12: Adjust duty ratio of A_8 at NA to 50 % Parameter GF1: Adjust duty ratio of B_8 at NB to 50 %

Table 61: Conditioning example 2

APPLICATION NOTES: CIRCUIT EXAMPLES

Refer to the datasheet of iC-MQ.

DESIGN REVIEW: Notes On Chip Functions

iC-MQF 3		
No.	Function, Parameter/Code	Description and Application Notes
1	SELRES, MTD	Recommended settings for resolution and minimum transition distance: STEP 400: $t_{MTD} \geq 125$ ns (MTD 0x4) STEP 800, 1000: $t_{MTD} \geq 175$ ns (MTD 0x6) STEP 2000: $t_{MTD} \geq 200$ ns (MTD 0x7) STEP 4000: $t_{MTD} \geq 300$ ns (MTD 0x8)
2	EMASKA, EMASKO, EMASKE	Error monitoring is not operational for: temporal tracking error, and loss of tracking; Mandatory programming: EMASKO(6) = 0. Allow driver reactivation by toggling bit END. EMASKO(7) = 0. Do not use driver shutdown for loss of tracking. EMASKE(6) = 0. Do not use error logging for configuration error. EMASKE(7) = 0, EMASKE(8) = 0. Do not use error logging for loss of tracking.
3	END	Recommended default programming of EEPROM: END = 1
4	ENZFF	Recommended default programming of EEPROM: ENZFF = 0. NB: ENZFF = 1 can blank index output if the external gating window is smaller than the selected AB cycle for indexing (adjusted by CFGZPOS).

Table 62: Chip release iC-MQF_3.

REVISION HISTORY

Rel.	Rel. Date*	Chapter	Modification	Page
A1	2013-11-08	...		

Rel.	Rel. Date*	Chapter	Modification	Page
B1	2014-06-16	FEATURES, THERMAL DATA	Standard operating temperature range extended to -40 to 100°C	1, 5
		ELECTRICAL CHARACTERISTICS	Item 201: AAabs changed to typ. 0.13° Items 601, 602: conditions simplified	7
		SERIAL CONFIGURATION INTERFACE	I^2C Slave Mode: text corrected, new subtitle: Intermediate error information buffer; Table 8, END: description corrected, parameter END represents Enable Device; Table 9 and 10, RAM Read/Write Access: correction of contents;	16
		SINE-TO-DIGITAL CONVERSION	Table 43, SELHYS: description improved	27
		ERROR MONITORING AND ALARM OUTPUT	Table 52, EPH: note supplemented Section Driver Shutdown: description supplemented; Table 58, EMASKO: correction of code description and notes; Section Error Protocol replaced by new section: Error Logging and Clearing ERR; Table 59, EMASKE, and Table 60 ERR: correction of contents;	31
		ORDERING INFORMATION	ET version removed (replaced by standard)	37

Rel.	Rel. Date*	Chapter	Modification	Page
C1	2015-10-14	ELECTRICAL CHARACTERISTICS	Item 514: Adaption of max. limit for condition MTD 0x02	8
		REGISTER MAP	Footnote edited for mandatory programming	14
		SERIAL CONFIGURATION INTERFACE	Tab. 8, END: Note edited	16
		OUTPUT SETTINGS AND ZERO SIGNAL	Tab. 42, CFGZPOS: Example supplemented Tab. 43, ENZFF: Note edited	28
		ERROR MONITORING AND ALARM OUTPUT	Tab. 56, EMASKO: Note edited Tab. 57, EMASKE: Note edited	31
		DESIGN REVIEW: Notes On Chip Functions	Update of contents	37

* Release Date format: *YYYY-MM-DD*

ORDERING INFORMATION

Type	Package	Order Designation
iC-MQF	TSSOP20	iC-MQF TSSOP20
Evaluation Board		iC-MQF EVAL MQ1D

Please send your purchase orders to our order handling team:

Fax: +49 (0) 61 35 - 92 92 - 692
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