iC-PN2656

PHASED ARRAY NONIUS ENCODER

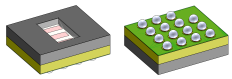
FEATURES

- Compact, 3-channel optical nonius encoder with differential scanning and analog sine/cosine outputs:
  255 CPR (N), 256 CPR (M), 240 CPR (S), size ⌀ 26 mm
- Phased-array design for excellent signal matching
- Reduced cross talk due to moderate track pitch
- Ultra low dark currents for operation up to high temperature
- Low noise amplifiers with high transimpedance gain
- Short-circuit-proof, low impedance voltage outputs for enhanced EMI tolerance
- Space saving optoQFN and optoBGA packages (RoHS compliant)
- Low power consumption from single 4.1 to 5.5 V supply
- Operational temperature range of -40 to +110 °C
- Suitable code discs:
  LSHC4S 26-256N (glass 1 mm)
  OD ⌀ 26 mm, ID ⌀ 11.6 mm, optical radius 10.905 mm
  LSHC5S 26-256N (plastic 1.15 mm),
  OD ⌀ 26 mm, ID ⌀ 7 mm, optical radius 10.905 mm

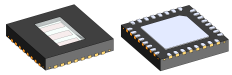
APPLICATIONS

- Absolute position encoders

PACKAGES

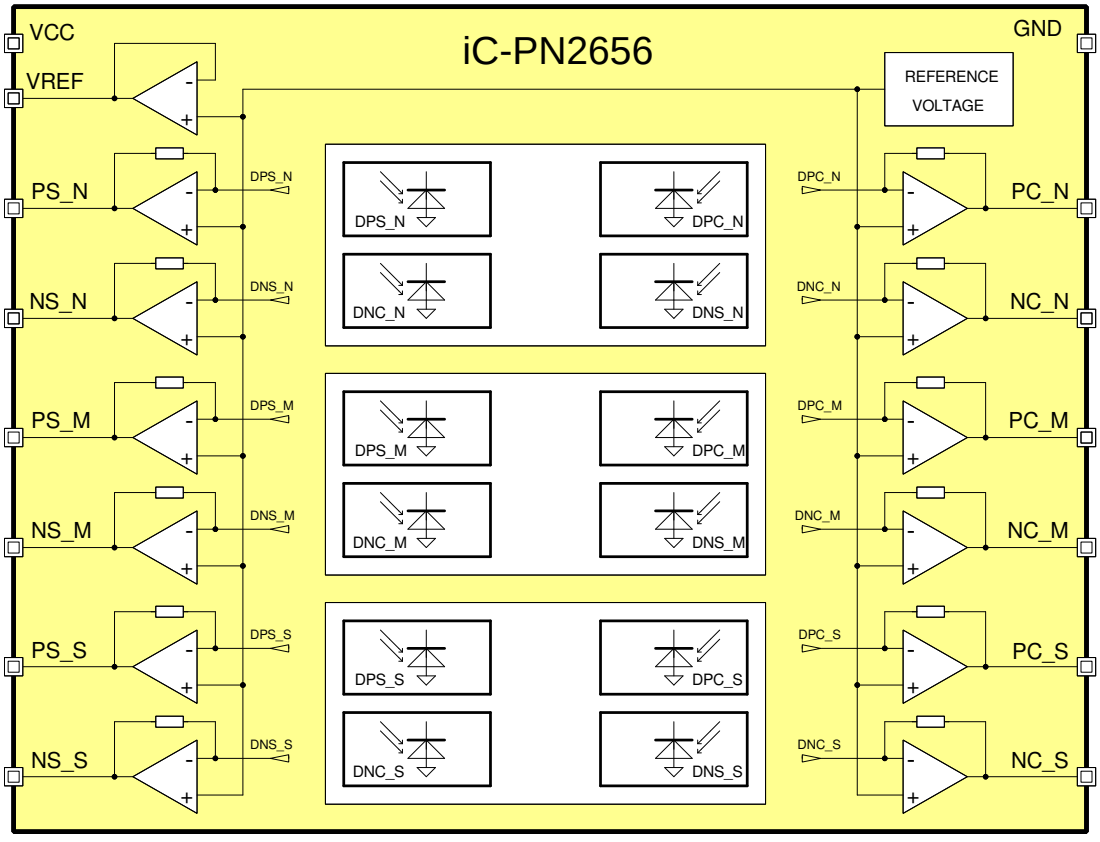


15-pin optoBGA
6.2 mm x 5.2 mm x 1.7 mm



32-pin optoQFN
5 mm x 5 mm x 0.9 mm

BLOCK DIAGRAM



DESCRIPTION

The optical encoder iC-PN2656 features monolithically integrated photosensors arranged as a phased-array.

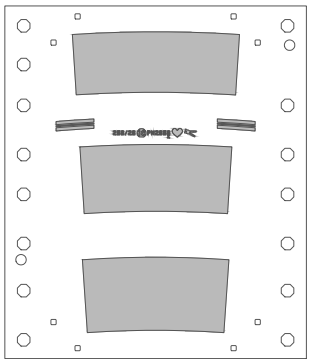
A high transimpedance gain of typically 1 MΩ generates output signals of a few hundred millivolt already from illumination levels of 3 mW/cm^2. In most cases no additional measures must be considered to filter for noise and interferences.

Analog nonius encoders are the typical application for iC-PN2656. Its 3-track scanning features a phased-array of multiple photosensors each per track, generating positive and negative going sine signals, as well as positive and negative going cosine signals. An excellent matching and common mode behavior of the differential signal paths is obtained by a paired amplifier design, reducing the needs for external signal calibration to an absolute minimum.

HD Phased Arrays are designed for fidelity and robustness. Ultra-low signal distortion is obtained at increased tolerances for alignment and random code defects (e.g. due to dust).
For information on chip releases, refer to chapter Design Review.

PACKAGING INFORMATION

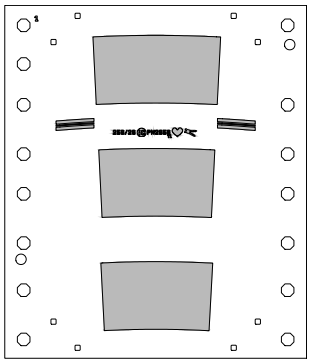
PAD LAYOUT
Chip release Z (2.88 mm x 3.37 mm)



PAD FUNCTIONS

No.	Name	Function
		Refer to the description of pin functions.
		Grey sections represent sensor layout areas; fill factors vary.

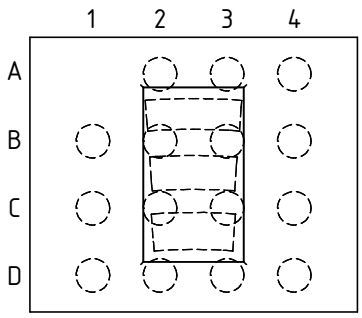
PAD LAYOUT
Chip release Y1 (2.88 mm x 3.37 mm),
HD Phased Array



PAD FUNCTIONS

No.	Name	Function

PIN CONFIGURATION
oBGA LSH2C (6.2 mm x 5.2 mm)

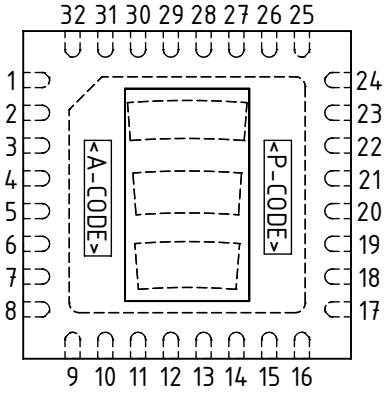


PIN FUNCTIONS

No.	Name	Function
A2	VCC	+4.1..5.5 V Supply Voltage
A3	VREF	Reference Voltage Output
A4	GND	Ground
B1	PS_N	N-Track Sine +
B2	NS_N	N-Track Sine -
B3	NC_N	N-Track Cosine -
B4	PC_N	N-Track Cosine +
C1	PS_M	M-Track Sine +
C2	NS_M	M-Track Sine -
C3	NC_M	M-Track Cosine -
C4	PC_M	M-Track Cosine +
D1	PS_S	S-Track Sine +
D2	NS_S	S-Track Sine -
D3	NC_S	S-Track Cosine -
D4	PC_S	S-Track Cosine +
		Note: All signal outputs are analog voltage outputs.

For dimensional specifications refer to the relevant package data sheet, available separately.

PIN CONFIGURATION
oQFN32-5x5 (5 mm x 5 mm)

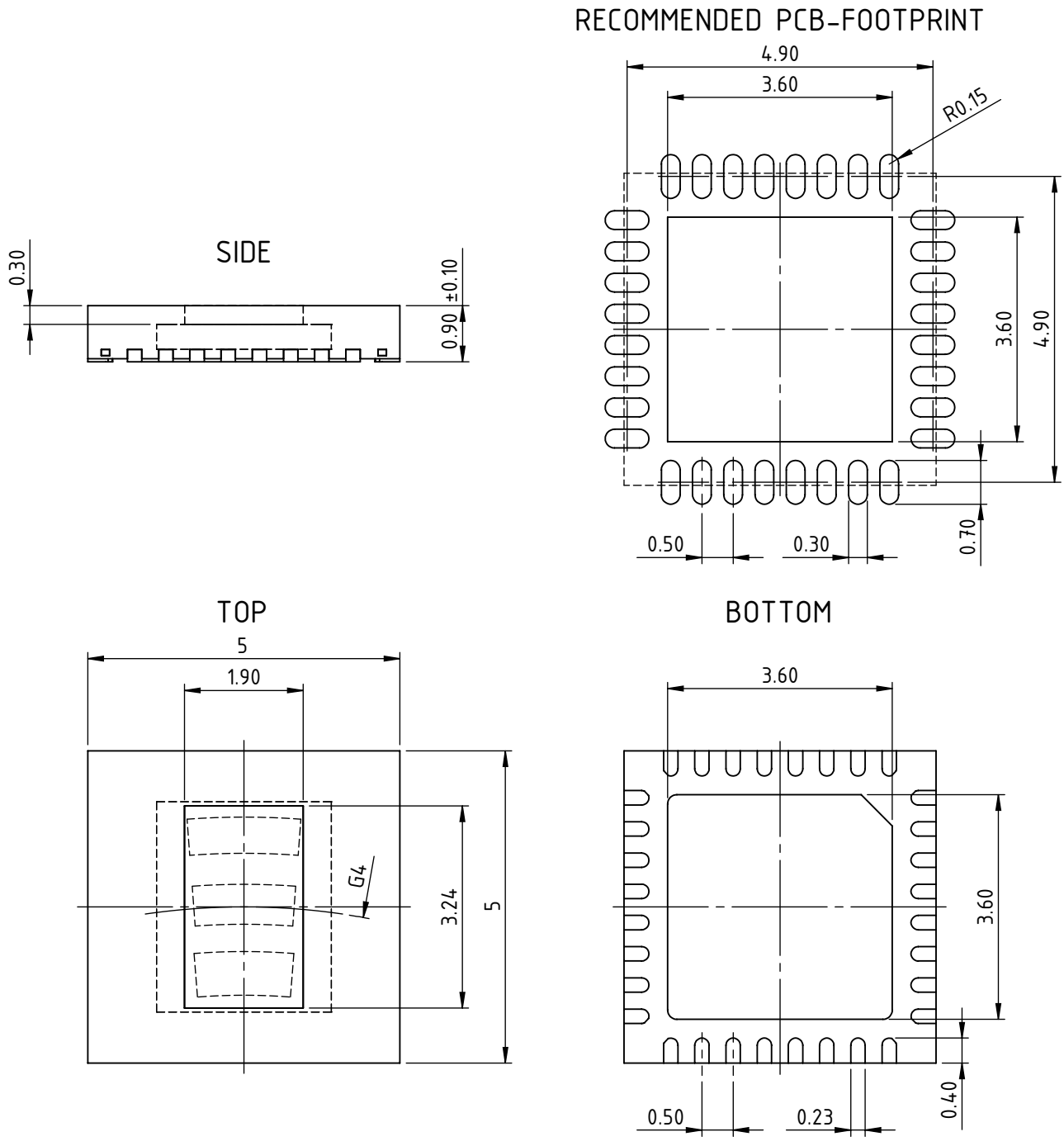


PIN FUNCTIONS

No.	Name	Function
1	VCC	+4.1..5.5 V Supply Voltage
2	VREF	Reference Voltage Output
3	PS_N	N-Track Sine +
4	NS_N	N-Track Sine -
5	PS_M	M-Track Sine +
6	NS_M	M-Track Sine -
7	PS_S	S-Track Sine +
8	NS_S	S-Track Sine -
9..16	n.c.[1)]	
17	NC_S	S-Track Cosine -
18	PC_S	S-Track Cosine +
19	NC_M	M-Track Cosine -
20	PC_M	M-Track Cosine +
21	NC_N	N-Track Cosine -
22	PC_N	N-Track Cosine +
24	GND	Ground
25..32	n.c.[1)]	
	BP	Backside paddle [2)]
		Note: All signal outputs are analog voltage outputs.

IC top marking: <P-CODE> = product code, <A-CODE> = assembly code (subject to changes);
1) Pin numbers marked n.c. are not connected.
2) Connecting the backside paddle is recommended by a single link to GND. A current flow across the paddle is not permissible.

PACKAGE DIMENSIONS oQFN32-5x5



All dimensions given in mm. Tolerances of form and position according to JEDEC MO-220.
Positional tolerance of sensor pattern: ±70µm / ±1° (with respect to backside pad).
G4: radius of chip center (refer to the relevant encoder disc and code description).
Maximum molding excess +20µm / -75µm versus surface of glass/reticle.

drb_pnxx-oqfn32-2_pack_1, 10:1

ABSOLUTE MAXIMUM RATINGS

These ratings do not imply operating conditions; functional operation is not guaranteed. Beyond these ratings device damage may occur.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	VCC	Voltage at VCC		-0.3	6	V
G002	I(VCC)	Current in VCC		-20	20	mA
G003	V()	Pin Voltage, all signal outputs		-0.3	VCC + 0.3	V
G004	I()	Pin Current, all signal outputs		-20	20	mA
G005	Vd()	ESD Susceptibility, all pins	HBM, 100 pF discharged through 1.5 kΩ		2	kV
G006	Tj	Junction Temperature		-40	150	°C
G007	Ts	Chip Storage Temperature		-40	150	°C

THERMAL DATA

Operating conditions: VCC = 4.1...5.5 V

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range	package oQFN32-5x5 package oBGA LSH2C (extended temperature range on request)	-40 -40		110 110	°C °C
T02	Ts	Storage Temperature Range	package oQFN32-5x5 package oBGA LSH2C	-40 -40		110 110	°C °C
T03	Tpk	Soldering Peak Temperature	package oQFN32-5x5 tpk < 20 s, convection reflow tpk < 20 s, vapor phase soldering MSL 5A (max. floor live 24 h at 30 °C and 60 % RH); Please refer to customer information file No. 7 for details.			 245 230	 °C °C
T04	Tpk	Soldering Peak Temperature	package oBGA LSH2C tpk < 20 s, convection reflow tpk < 20 s, vapor phase soldering TOL (time on label) 8 h; Please refer to customer information file No. 7 for details.			 245 230	 °C °C

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating conditions: VCC = 4.1...5.5 V, Tj = -40..125 °C, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device							
001	VCC	Permissible Supply Voltage		4.1		5.5	V
002	I(VCC)	Supply Current in VCC	no load, photocurrents within linear op. range (no override)		9.5	15	mA
003	Vc()hi	Clamp-Voltage hi at all pins	I() = 4 mA			11	V
004	Vc()lo	Clamp-Voltage lo at all pins	I() = -4 mA	-1.2		-0.3	V
Photosensors							
101	λar	Spectral Application Range	Se(λar) = 0.25 x S(λpk)	400		950	nm
102	λpk	Peak Sensitivity Wavelength			680		nm
103	Aph()	Radiant Sensitive Area	chip release PN2656_Z chip release PN2656_Y1		0.11 0.12		mm^2 mm^2
104	S(λ)	Spectral Sensitivity	λ_{LED} = 740 nm λ_{LED} = 850 nm		0.45 0.30		A/W A/W
106	E()mxr	Irradiance For Maximum Signal Level	λ_{LED} = 740 nm, Vout() not saturated; chip release PN2656_Z chip release PN2656_Y1		6.4 4.6		mW/cm^2 mW/cm^2
Photocurrent Amplifiers							
201	Iph()	Permissible Photocurrent Operating Range		0		1120	nA
202	η()r	Photo Sensitivity (light-to-voltage conversion ratio)	λ_{LED} = 740 nm; chip release PN2656_Z chip release PN2656_Y1	0.2	0.28 0.28	0.5	V/µW V/µW
203	Z()	Equivalent Transimpedance Gain	Z = Vout() / Iph()	0.7	1.0	1.4	MΩ
204	TCz	Temperature Coefficient of Transimpedance Gain			-0.12		%/°C
209	ΔZ()pn	Transimpedance Gain Matching	P.. channel vs. corresponding N.. channel	-0.2		0.2	%
210	ΔVout()pn	Signal Matching	no illumination, any output vs. any output	-35		35	mV
211	ΔVout()pn	Signal Matching	no illumination, P.. output vs. corresponding N.. output	-2.5		2.5	mV
212	fc()hi	Cut-off Frequency (-3 dB)			400		kHz
213	VNoise()	RMS Output Noise	illuminated to 500 mV signal level above dark level, 500 kHz band width		0.5		mV
Signal Outputs							
301	Vout()mx	Permissible Maximum Output Voltage	illumination to E()mxr, linear gain; VCC = 4.5...5.5 V VCC = 4.1 V	2.45 2.05	2.72 2.3	3.02 2.6	V V
302	Vout()d	Dark Signal Level	no illumination, load 20 kΩ vs. +2 V	575	770	1000	mV
303	Vout()acmx	Maximum Signal Level	Vout()acmx = Vout()mx - Vout()d; VCC = 4.5...5.5 V VCC = 4.1 V	1.48 1.18	1.96	2.35 2.35	V V
304	Isc()hi	Short-Circuit Current hi	load current to ground	100	420	1000	µA
305	Isc()lo	Short-Circuit Current lo	load current to IC	250	480	700	µA
306	Ri()	Internal Output Resistance	f = 1 kHz	70	110	180	Ω
307	ton()	Power-On Settling Time	VCC = 0 V → 5 V			100	µs
Reference Voltage VREF							
401	VREF	Reference Voltage	I(VREF) = -100...+300 µA	575	770	1000	mV
402	dVout()	Load Balancing	I(VREF) = -100...+300 µA	-10		+10	mV
403	Isc()hi	Short-Circuit Current hi	load current to ground	200	420	1400	µA
404	Isc()lo	Short-Circuit Current lo	load current to IC	0.4	4.5	10	mA

APPLICATION CIRCUITS

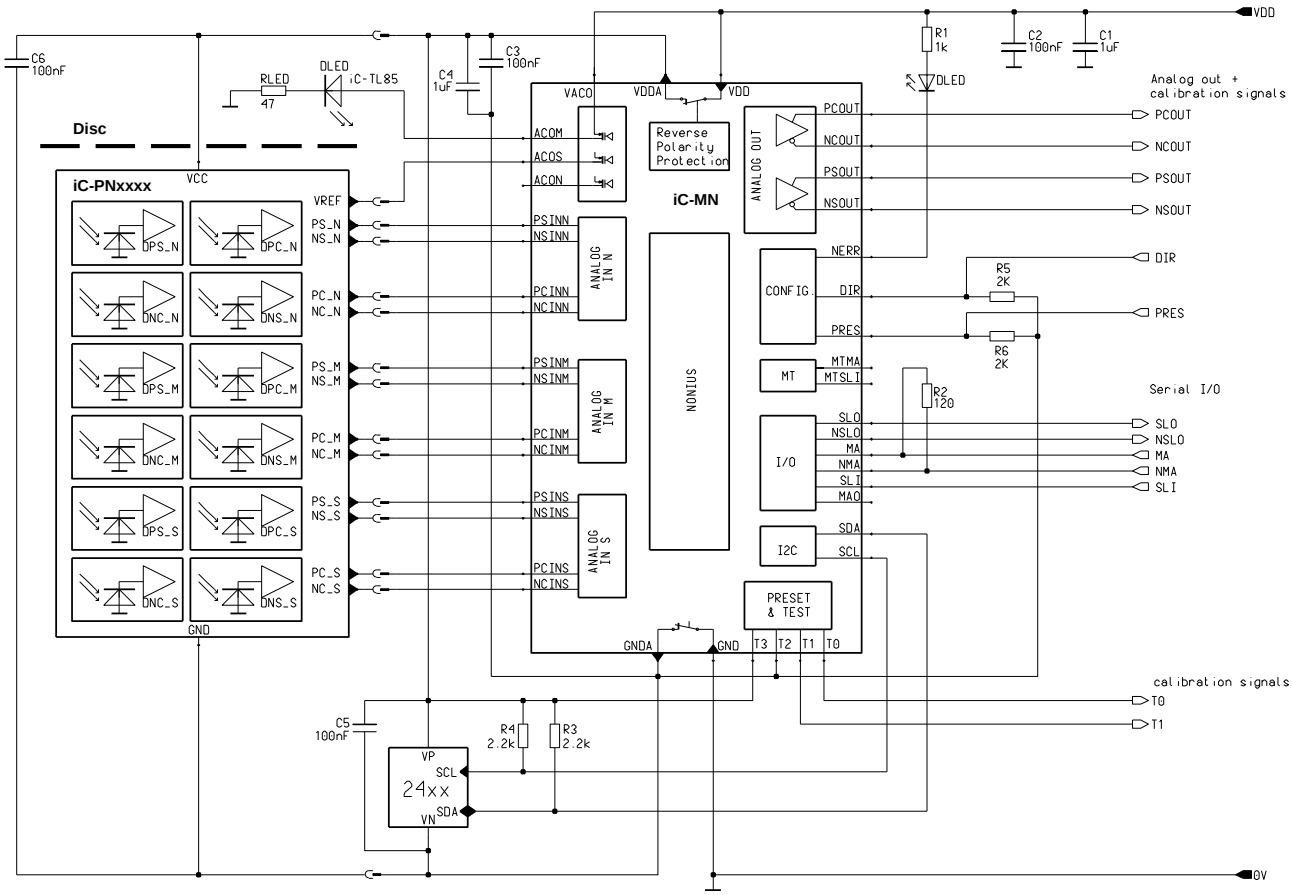


Figure 1: Application example of absolute encoder circuit.

DESIGN REVIEW: Notes On Chip Functions

iC-PN2656 2		
No.	Function, Parameter/Code	Description and Application Hints
1		Please refer to former datasheet release C2.

Table 4: Notes on chip functions regarding iC-PN2656 chip release 2

iC-PN2656 Z		
No.	Function, Parameter/Code	Description and Application Hints
1		None at time of printing (datasheet release C2, 2013). Changes to Elec. Char. are documented by this datasheet release, including the extension of operating voltage down to 4.1 V (safe by design).

Table 5: Notes on chip functions regarding iC-PN2656 chip release Z

iC-PN2656 Y1		
No.	Function, Parameter/Code	Description and Application Hints
1	*HD Phased Array*	Chip release utilizes a high density phased array layout. Improvement of alignment marks: enlarged radial size, inner ring omitted.

Table 6: Notes on chip functions regarding iC-PN2656 chip release Y1.

REVISION HISTORY

Rel	Rel.Date	Chapter	Modification	Page
C2	13-10-28	...		

Rel	Rel.Date	Chapter	Modification	Page
D1	14-09-05	FEATURES	Supply voltage extended to include 4.1 V	1
		DESCRIPTION	Description of *HD Phased Array* supplemented	2
		PACKAGING INFORMATION	Chip release Y1 supplemented, oQFN package drawings updated for top marking and tolerances	2, 3
		ELECTRICAL CHARACTERISTICS	Operating conditions: VCC supply voltage extended to include 4.1 V Item 001: min. limit; item 101, condition: reference is λpk; Items 103, 106, 202: update of values for Z and Y1 chip releases Items 201, 203, 212: update of values for Z and Y1 chip releases Items 301, 303: conditions and limits for 4.1 V; Item 302, 401: min. limit; item 304, 403: max. limit;	6
		DESIGN REVIEW: Notes On Chip Functions	Chapter supplemented	8
		ORDERING INFORMATION	Update of P/O codes and items	9

ORDERING INFORMATION

Type	Package	Options	Order Designation
iC-PN2656	32-pin optoQFN, 5 mm x 5 mm, thickness 0.9 mm RoHS compliant		iC-PN2656 oQFN32-5x5
	15-pin optoBGA, 6.2 mm x 5.2 mm, thickness 1.7 mm RoHS compliant		iC-PN2656 oBGA LSH2C
Evaluation Kit	PCB (60 mm x 40 mm), assembled with optoQFN	with LED and code disc	iC-PN2656 EVAL PNH1M
	PCB (60 mm x 40 mm), assembled with optoBGA	with LED and code disc	iC-PN2656 EVAL LSH2M
Code Discs		255/256/240 PPR OD ∅ 26 mm, ID ∅ 11.6 mm, optical radius 10.905 mm (glass 1 mm)	LSHC4S 26-256N
		255/256/240 PPR OD ∅ 26 mm, ID ∅ 7 mm, optical radius 10.905 mm (plastic 1.15 mm)	LSHC5S 26-256N

For technical support, information about prices and terms of delivery please contact:

iC-Haus GmbH
Am Kuemmerling 18
D-55294 Bodenheim
GERMANY

Tel.: +49 (0) 61 35 - 92 92 - 0
Fax: +49 (0) 61 35 - 92 92 - 192
Web: http://www.ichaus.com
E-Mail: sales@ichaus.com

Appointed local distributors: http://www.ichaus.com/sales_partners