iC-NZP

P-TYPE LASER DIODE DRIVER

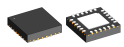
FEATURES

- Peak value controlled laser driver for operation from CW up to 155 MHz
- Spike-free switching of laser currents of up to 300 mA
- Setting of laser power (APC) via external resistor
- Optional current control (ACC)
- Laser current limitation
- LVDS/TTL switching input with TTL monitor output
- Low current consumption sleep-mode < 50 µA
- Safety shutdown with overtemperature
- Error signal output with overtemperature, undervoltage and overcurrent
- All current LD types can be used (P/M/N configurations)
- Fast soft-start
- Strong suppression of transients with small external capacitors

APPLICATIONS

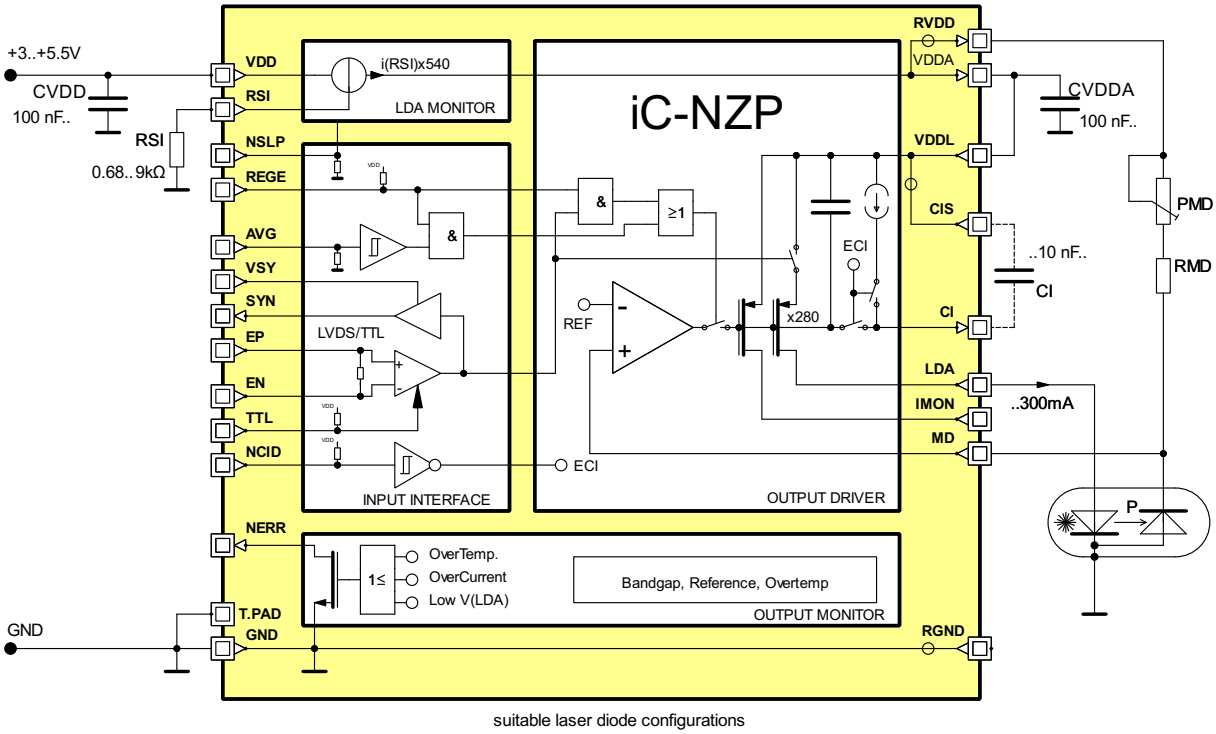
- Pulsed and CW laser diode modules
- Laser diode pointers
- Laser levels
- Bar-code readers
- Distance measurement

PACKAGES



QFN24
4 mm x 4 mm

BLOCK DIAGRAM



DESCRIPTION

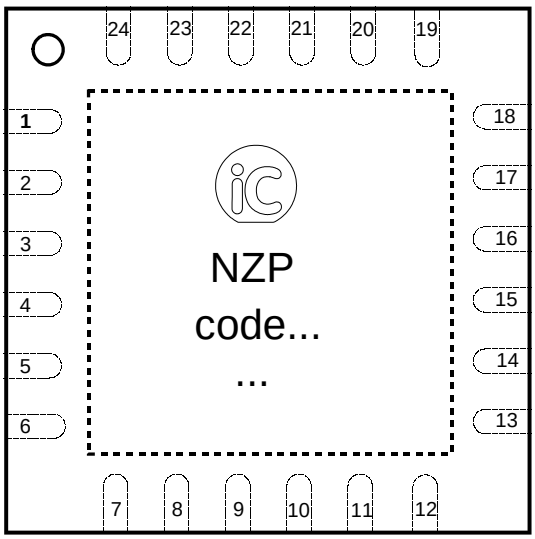
Laser diode pulse driver iC-NZP allows CW operation of laser diodes and spike-free switching with defined current pulses up to 155 MHz. The optical output power of the laser diode is set-up by means of an external resistor (RMD/PMD). For laser current control without a monitor diode, the laser current monitor at pin IMON is utilised. For high pulse frequencies the device can be switched into controlled *burst mode*. A previously settled operating point is maintained throughout the burst phase.

An averaging current monitor can be set by an external resistor at pin RSI. When the current limit is reached, overcurrent is signalled at NERR and the current from pin VCCA is limited to the pre-set value but the iC is not shut down. There is an additional current limitation in pin LDA that prevents the iC from overpowering the laser diode.

Setting pin NSLP low, the iC enters a low consumption sleep-mode (< 50 µA typ.).

PACKAGING INFORMATION QFN24 4 mm x 4 mm to JEDEC

PIN CONFIGURATION



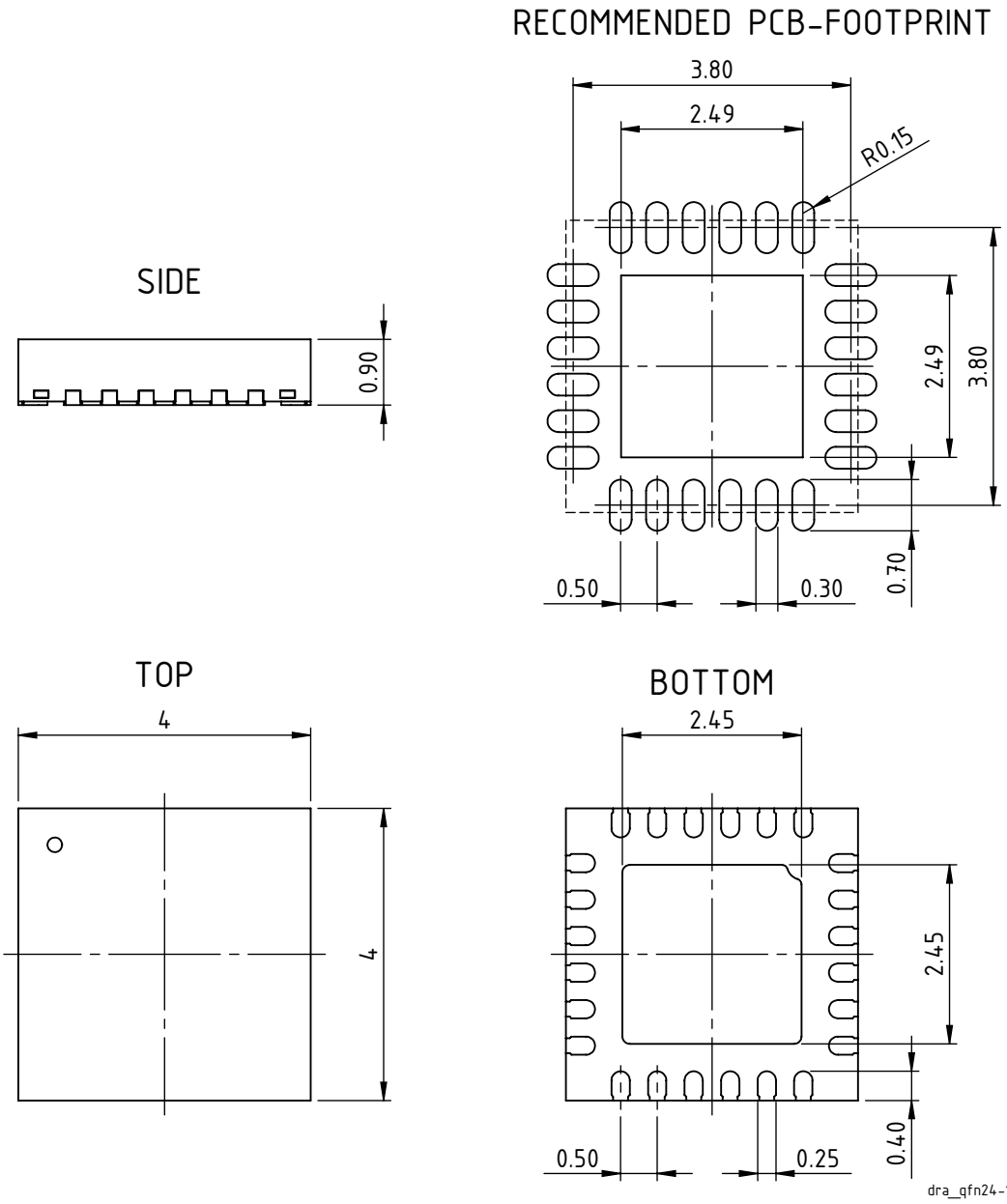
PIN FUNCTIONS

No.	Name	Function
1	VDD	Power Supply
2	GND	Ground
3	MD	APC setup, monitor input
4	IMON	Laser Current Monitor
5	NCID	Disable Pulldown Current at CI
6	EP	Positive LVDS/TTL switching input
7	EN	Negative LVDS switching input
8	TTL	Enable TTL input
9	VSY	Sync Output Supply Voltage
10	SYN	Sync Output
11	RGND	Reference Ground
12	RVDD	Reference (P-type laser diodes)
13	LDA	Laser Diode Anode
14	CI	Power Control Capacitor
15	CIS	Power Control Capacitor sense
16	VDDL	Laser Power Supply
17	VDDA	Analogue Power Supply
18	AVG	Averaging Control Enabled
19	RSI	Current Monitor Setup
20	REGE	Control Enable
21	GND	Ground
22	NSLP	Not Sleep-Mode
23	NERR	Error Output
24		n/c

The *Thermal Pad* is to be connected to a Ground Plane (GND) on the PCB.
Only pin 1 marking on top or bottom defines the package orientation (iC NZP label and coding is subject to change).

PACKAGE DIMENSIONS

All dimensions given in mm.



ABSOLUTE MAXIMUM RATINGS

Beyond these values damage may occur; device operation is not guaranteed.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	VDD	Voltage at VDD		-0.7	6	V
G002	I(VDD)	Current in VDD	DC current	-2	1200	mA
G003	I(CI)	Current in CI	V(LDA) = 0	-2	5	mA
G004	I(NERR)	Current in NERR		-2	20	mA
G005	I(MD)	Current in MD		-2	20	mA
G006	I()dig	Current in EP, EN, TTL, REGE, NSLP, AVG, NCID		-2	20	mA
G007	I(VDDL)	Current in VDDL	DC current	-2	1200	mA
G008	I(VDDA)	Current in VDDA	DC current	-1200	2	mA
G009	I(LDA)	Current in LDA	DC current	-1200	2	mA
G010	I(RSI)	Current in RSI		-2	20	mA
G011	I(VSY)	Current in VSY		-2	50	mA
G012	I(SYN)	Current in SYN		-2	50	mA
G013	I(IMON)	Current in IMON		-20	2	mA
G014	V()c	Voltage at RSI, VSY, SYN, EP, EN, TTL, REGE, AVG, NCID, RGND, MD, CI, IMON, RVDD, LDA, NERR, NSLP		-0.7	6	V
G015	Vd()	ESD Susceptibility at all pins	HBM, 100 pF discharged through 1.5 kΩ		2	kV
G016	Tj	Operating Junction Temperature		-40	190	°C
G017	Ts	Storage Temperature Range		-40	190	°C

THERMAL DATA

Operating Conditions: VDD = 3...5.5 V

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range (extended range on request)		-20		85	°C
T02	Rthja	Thermal Resistance Chip/Ambient	surface mounted, thermal pad soldered to ca. 2 cm² heat sink		30	40	K/W

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 3...5.5 V, VSY = 0 V...VDD, Tj = -40...85 °C, NSLP = hi, NCID = hi; unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device							
001	VDD	Permissible Supply Voltage		3		5.5	V
002	VSY	Permissible Supply Voltage at VSY	VSY ≤ VDD	3		5.5	V
003	Ioff(VDD)	Supply Current in VDD	NSLP = lo, all other input pins set to lo		5	50	µA
004	Idc(VDD)	Supply Current in VDD	RSI ≥ 680 Ω		10	15	mA
005	I(VSY)	Supply Current in VSY	SYN pin open			10	µA
006	Toff	Thermal Shutdown Threshold		130		196	°C
007	VDDon	Power-On Threshold		1.7		2.8	V
008	Vc()hi	Clamp Voltage hi at RSI, TTL, REGE, MD, CI, LDA, VDDA, VDDL, NSLP, IMON, NCID, AVG	I() = 0.1 mA, other pins open, VDD = 0	0.3		1.6	V
009	Vc(SYN)hi	Clamp Voltage hi to VSY	I() = 1 mA, other pins open, VSY = 0	0.3		1.5	V
010	Vc()lo	Clamp Voltage lo at VDD, AVG, MD, IMON, NCID, EP, EN, TTL, VSY, SYN, RVDD, VDDL, VDDA, CI, LDA, RSI, REGE, NSLP, NERR	I() = -1 mA, other pins open	-1.5	-0.65	-0.3	V
011	Vc(VSY)hi	Clamp Voltage hi at VSY	I() = 1 mA, other pins open, VDD = 0			6	V
Current Monitor RSI, VDDA, VDDL, LDA							
101	V(RSI)	Voltage at RSI		420	500	580	mV
102	RSI	Permissible Resistor at RSI	VDD = 3...3.5 V VDD = 4.5...5.5 V	2.5 0.68		9 9	kΩ kΩ
104	V(VDDL)	Permissible voltage at VDDL	When not connected to VDDA	0		V(VDD)	
106	Cmin()	Minimum capacitor required at VDDA		100			nF
107	rIVDDA	Current Ratio I(VDDA)max / I(RSI)	V(VDDA) = 0 V; VDD = 4.5...5.5 V VDD = 3...3.5 V		550 525		
108	rILDA	Current Ratio I(LDA)max / I(RSI)	V(REGE) = V(TTL) = V(EP) = VDD, V(LDA) = 0 V, V(MD) = 0; VDD = 4.5...5.5 V VDD = 3...3.5 V		520 500		
109	i(LDA)	Maximum limited current	RSI = 680 Ω, VDD = 5.5 V	-630			mA
110	Rdis()	Discharge Resistor at VDDA	NSLP = lo, V(VDDA) = VDD	1		20	kΩ
Reference							
201	V(MD)	Reference Voltage	V(MD) – V(RGND), V(RVDD) – V(MD) for P-type LD, closed control loop	210	250	320	mV
202	dV(MD)	Temperature Drift of Voltage at MD	closed control loop		120		µV/°C
203	V(MD)	Precharge Reference Voltage	V(RVDD) – V(MD); V(EP) = 0, V(AVG) = 0, P-type MD	230	280	390	mV
Digital Inputs/Outputs							
301	Vin()	Input Voltage Range at EP, EN	TTL = lo, VDD = 3.0...5.5 V	0.6		VDD – 1.4	V
302	Vd()	Input Differential Voltage at EP, EN	TTL = lo, Vd() = |V(EP) – V(EN)|	200			mV
303	R()	Differential Input Impedance at EP, EN	V(EP), V(EN) < VDD – 1.5 V, TTL = lo	0.6		3	kΩ
304	Vt(EP)hi	Input Threshold Voltage hi at EP	TTL = hi, EN = open			2	V
305	Vt(EP)lo	Input Threshold Voltage lo at EP	TTL = hi, EN = open	0.8			V
306	Vhys(EP)	Hysteresis at EP	TTL = hi, EN = open	40			mV
307	Ipd(EP)	Pull-Down Current at EP	TTL = hi, EN = open, V() = 1 V...VDD	0.5		5	µA

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 3...5.5 V, VSY = 0 V...VDD, Tj = -40...85 °C, NSLP = hi, NCID = hi; unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
308	Vt()hi	Input Threshold Voltage hi at TTL, REGE, NSLP, AVG, NCID				2	V
309	Vt()lo	Input Threshold Voltage lo at TTL, REGE, NSLP, AVG, NCID		0.8			V
310	Vhys()	Hysteresis at TTL, REGE, NSLP, AVG, NCID		130	230		mV
311	Ipu()	Pull-Up Current at TTL, REGE, NCID	V() = 0...VDD − 1.2 V	-60		-2	µA
312	Ipd()	Pull-Down Current at NSLP, AVG	V() = 1 V...VDD	2		130	µA
313	Vs()hi	Saturation voltage hi at SYN	Vs(SYN)hi = VSY − V(SYN), I() = -1 mA, VSY = VDD, EP = TTL = hi, EN = open			0.4	V
314	Vs()lo	Saturation voltage lo at SYN	I() = 1 mA, VSY = VDD, TTL = hi, EP = lo, EN = open			0.4	V
315	Isc()hi	Short-circuit Current hi at SYN	EP = TTL = hi, EN = open, V(SYN) = 0 V, VSY = VDD	-40		-3	mA
316	Isc()lo	Short-circuit Current lo at SYN	TTL = hi, EP = lo, EN = open, V(SYN) = VSY, VSY = VDD	3		40	mA
317	I(NERR)	Current in NERR	V(NERR) > 0.6 V, error	1		20	mA
318	Vs()lo	Saturation Voltage lo at NERR	I() = 1 mA, error			600	mV
Laser Driver LDA, CI, IMON							
401	Vs(LDA)hi	Saturation Voltage hi at LDA	Vs(LDA)hi = V(VDDL) − V(LDA); RSI = 680 Ω I(LDA) = 300 mA, VDD = 4.5...5.5 V I(LDA) = 100 mA, VDD = 4.5...5.5 V I(LDA) = 60 mA, RSI = 2.5 kΩ VDD = 3...3.5 V		 1.6 1.2 0.8	 2.2 2 1.3	 V V V
402	Idc(LDA)	Permissible DC Current in LDA		-300			mA
403	C(CI)	Required Capacitor at CI		0	10		nF
404	|I(CI)|	Charge Current from CI	iC active, REGE = hi, V(VDD) − V(CI) = 1 V; NCID = hi NCID = lo	 20	 0	 60	 µA µA
405	Ipu(CI)	Pull-Up Current in CI	iC active, REGE = NCID = lo, V(CI) = 0 V...VDD − 1 V	-2.6		-0.3	µA
406	Imon()	Current at IMON	V(IMON)=0.5V; I(LDA) < 100 mA, VDD = 3...4.5 V I(LDA) < 300 mA, VDD = 4.5...5.5 V	1/330		1/210	I(LDA)
Timing							
501	twu	Time to Wakeup: NSLP lo → hi to system enable	CVDDA = 1 µF, RSI = 1 kΩ			300	µs
502	tr	Laser Current Rise Time	VDD = 5 V see Fig. 2			1.5	ns
503	tf	Laser Current Fall Time	VDD = 5 V see Fig. 2			1.5	ns
504	tp	Propagation Delay V(EPx, ENx) → I(LDAx)	VDD = 5 V			10	ns

ELECTRICAL CHARACTERISTICS: DIAGRAMS

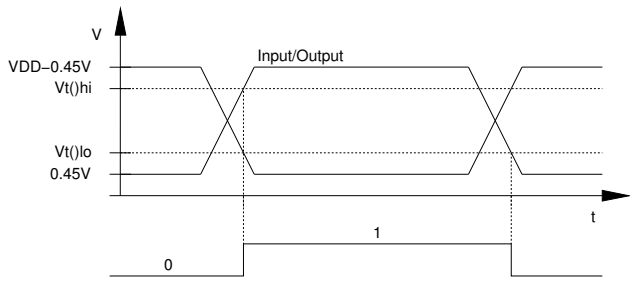


Figure 1: Reference levels

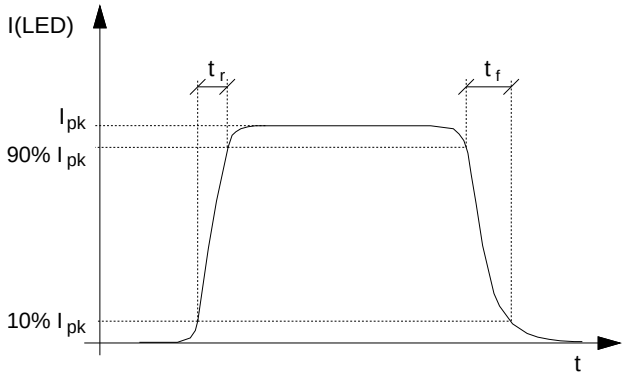


Figure 2: Laser current pulse

DESCRIPTION OF FUNCTIONS

iC-NZP is a laser diode pulse driver, which features:

- Averaging or peak control
- Optical power or current control
- Laser current limitation
- Pulses of up to 155 MHz in controlled *burst mode*
- Sleep mode with less than 50 µA consumption
- Error signalling for overcurrent

OPTICAL POWER CONTROL

The iC-NZP supports the control of the laser diode's optical output power (APC) for all common laser diode pin configurations (P, N and M). The control is enabled with pin REGE set to high. With AVG set to low, the peak power control is enabled. The laser power level is selected by means of the resistor RMON (= RMD + PMD). This control mode can be used for frequencies up to ca. 4 Mhz. For higher frequencies the averaging control (AVG = high) or the *burst mode* have to be used.

Tables 4 and 5 show how to set the inputs for laser control depending on the input interface selected (TTL or LVDS).

Laser control in TTL mode (TTL = high/open)					
EP	**EN**	**NSLP**	**REGE**	**SYN**	**Mode**
-	-	low/open	-	-	Power-save mode
low/open	open	high	-	low	VDDA charged, laser off
high	open	high	high/open	high	VDDA charged, laser on, regulated
high	open	high	low	high	VDDA charged, laser on, burst mode

Table 4: Laser control in TTL mode

Laser control in LVDS mode (TTL = low)					
EP	**EN**	**NSLP**	**REGE**	**SYN**	**Mode**
-	-	low/open	-	-	Power-save mode
< EN	> EP	high	-	low	VDDA charged, laser off
> EN	< EP	high	high/open	high	VDDA charged, laser on, regulated
> EN	< EP	high	low	high	VDDA charged, laser on, burst mode

Table 5: Laser control in LVDS mode

RMON dimensioning

Peak control (AVG = low): In order to calculate the right value of RMON, the value of *IM* (monitor current with respect to optical output power) of the laser diode must be known. RMON must be chosen in a way that the monitor current generated by the desired output power creates a voltage drop across RMON of 250 mV (cf. Electrical Characteristics No. 201).

Averaging control (AVG = high): In this mode the calculation is the same as in peak control, only the result has to be divided by the duty cycle of the laser pulses, $D = \frac{\tau}{T}$. At a duty cycle of e.g. 50% $D = \frac{1}{2}$.

Control modes		
Averaging	**Operation mode**	**RMON calculation**
AVG = 0	Peak control	$RMON = \frac{V(MD)}{IM}$
AVG = 1	Averaging control	$RMON = \frac{V(MD)}{IM \times D}$

Table 6: RMON dimensioning

Example
By way of example, an output level of 1 mW is to be set. With an optical power of 1 mW e.g. laser diode HL6342G has a typical monitor current (IM) of 15 µA. The following value is then obtained for the resistor at pin MD (RMON = PMD + RMD, where RMD is a fixed resistor and PMD a potentiometer.):

$$RMON = \frac{V(MD)}{IM} = \frac{0.25\,V}{15\,\mu A} = 16.67\,k\Omega$$

External capacitor mode
In applications where an external capacitor is required (see *best performance recommendations* below), the external capacitor mode must be enabled (pin NCID = low).

Best performance recommendations
The operating point for the laser diode is stored in an on-chip capacitor. This permits a fast start-up but can lead to an unstable control circuit under certain conditions such as inadequate PCB layout or laser with very low monitor current. In that cases, an external capacitor is to be connected as close as possible to the chip, across pin CI and CIS. This will prevent instability of the control circuit. For averaging control a 10 nF capacitor at CI is recommended. Special care must be taken in PCB layout when laying out the path from the laser diode's cathode to GND. This path must be kept as short as possible to avoid parasitic inductances. A *snubber network* across the laser diode also helps to compensate for these parasitic inductances.

Figures 3, 4 and 5 show the typical set-up for the different P, N and M-type diode configurations.

P-Type diodes

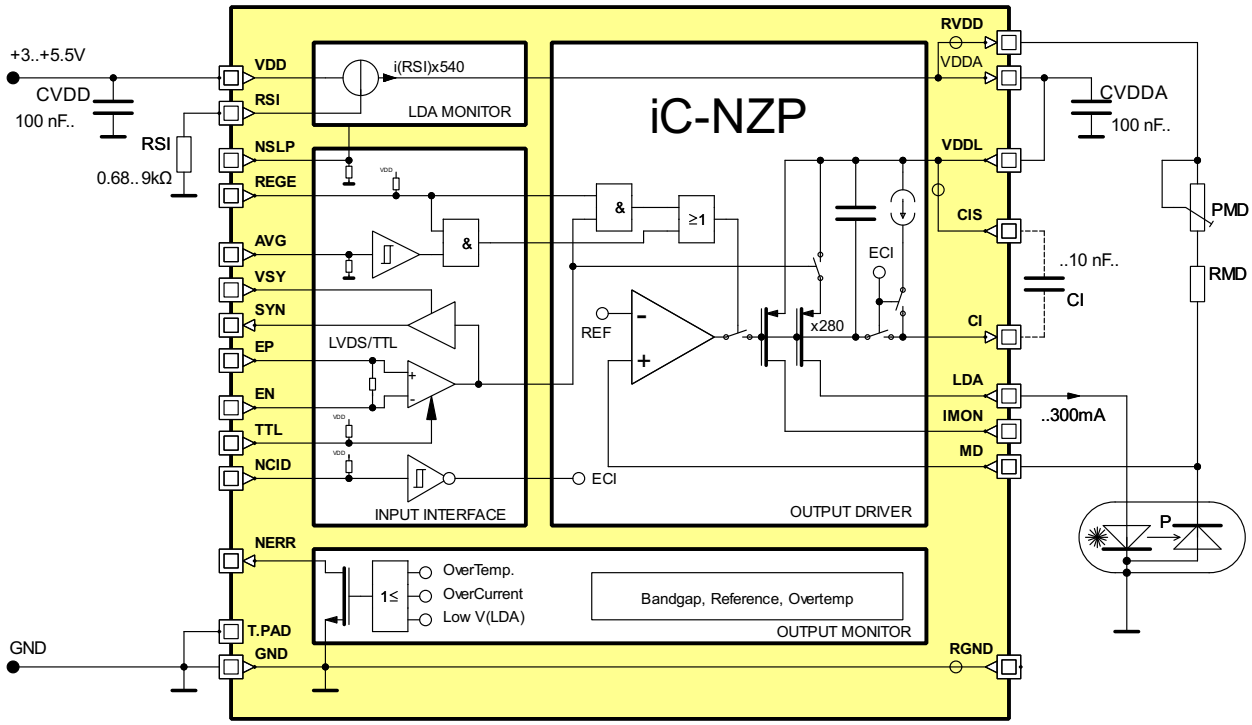


Figure 3: Circuit example for P-type laser diodes (case grounded)

M-Type diodes

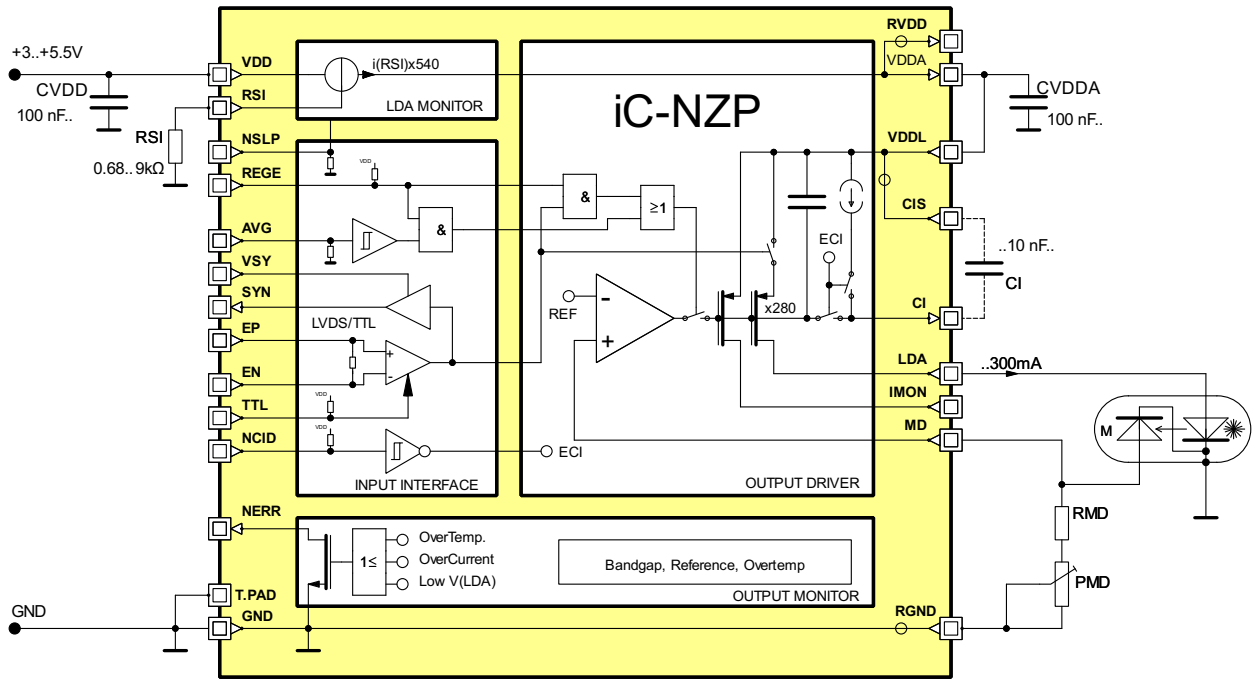


Figure 4: Circuit example for M-type laser diodes (case grounded)

N-Type diodes

Although this type of laser diodes are supported by iC-NZP, it's strongly recommended to use iC-NZN instead, since in this configuration all the pulses at LDA will be coupled directly to pin MD due to monitor photo diode's internal capacitance. Thus making an accurate control much more difficult.

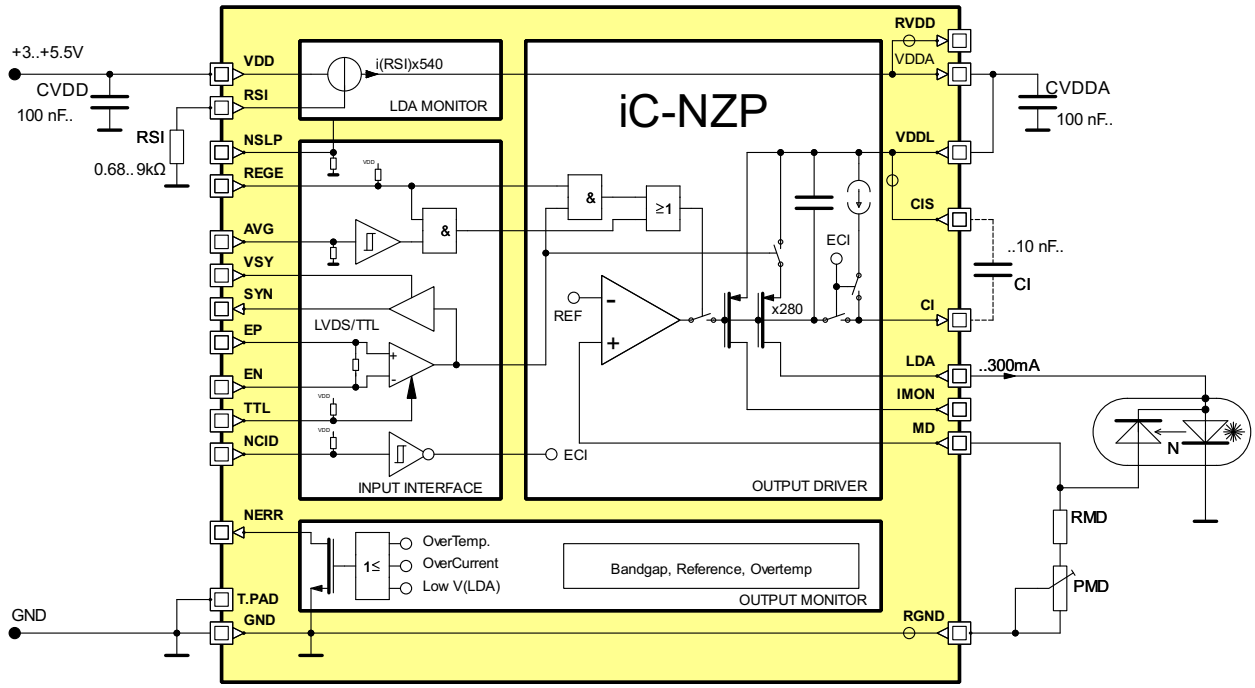


Figure 5: Circuit example for N-type laser diodes

LASER CURRENT LIMITATION

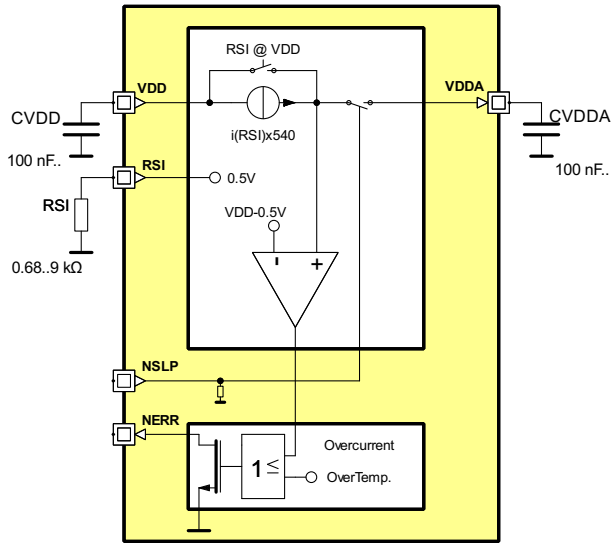


Figure 6: iC-NZP VDDA current limitation

iC-NZP monitors the average laser current flowing from pin VDDA (Figure 6). The DC current limit is set by means of a resistor at pin RSI.

When dimensioning resistor RSI the following applies (cf. Electrical Characteristics No. 107):

$$I_{max}(VDDA) = 540 \times \frac{0.5\,V}{RSI}$$

Short pulses at VDDA with higher currents are possible as only the DC current is monitored and capacitor CVDDA supplies the current for short pulses.

BURST MODE

In *controlled burst mode* iC-NZP can pulse with up to 155 MHz. *Controlled* here means that a pre-set operating point is maintained during the *burst phase*.

Therefore an operating point is settled first, for which pin REGE has to be high and the laser must be switched on. Once the operating point has been reached the laser can be switched off again. The operating point is stored in an on-chip capacitor and when REGE is set to low, the *burst mode* is activated. The pre-set operating point is maintained. To prevent the laser current from rising due to residual currents, the capacitor is discharged with a maximum of 150 nA (cf. Electrical Characteristics No. 405). For a longer burst mode, an external capacitor can be connected to pin CI. As the capacitor is discharged gradually, the output level must be re-settled again after a certain period, depending on the admissible degradation of the laser output power.

CURRENT CONTROL

The iC-NZP also supports laser current control, when no monitor diode is present. For that purpose, a fraction of the current flowing trough the laser is provided at IMON pin (ILDA / 280, cf. Electrical Characteristics No. 406). The laser current is set by means of resistor RMON (= RMD + PMD).

$$RMON = \frac{V(MD)}{IMON}$$

Figure 7 shows the typical set-up for current control.

External capacitor mode
In applications where an external capacitor is required (see *best performance recommendations* below), the external capacitor mode must be enabled (NCID pin set to low).

Best performance recommendations
The operating point for the laser diode is stored in an on-chip capacitor. This permits a fast start-up but can lead to an unstable control circuit under certain conditions such as inadequate PCB layout or laser with very low monitor current. In that cases, an external capacitor is to be connected as close as possible to the chip, across pin CI and CIS. This will prevent instability of the control circuit.

Setting AVG to hi, keeps the control loop always on and settled, thus improving the dynamic performance.

Special care must be taken in PCB layout when laying out the path from the laser diode's cathode to GND. This path must be kept as short as possible to avoid parasitic inductances. A *snubber network* across the laser diode also helps to compensate for these parasitic inductances.

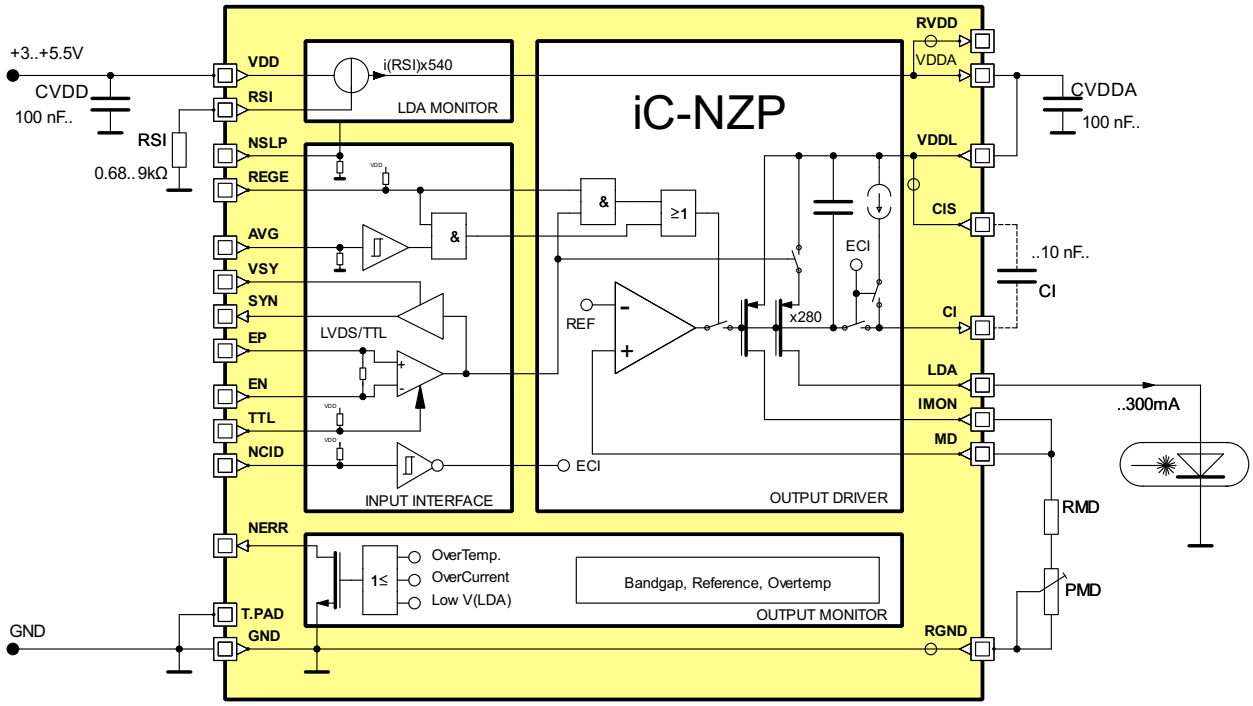


Figure 7: Example set-up for current control

SLEEP MODE

The iC-NZP has a very low consuption mode that permits hibernation in battery powered applications. Setting the NSLP pin to low drives the chip into a state where the VDDA pin is disconnected as supply and pulled down. The wake up from sleep time is about 300 µs

EVALUATION BOARD

iC-NZP comes with an evaluation board for test purpose. Figures 8 and 9 show both the schematic and the component side of the evaluation board.

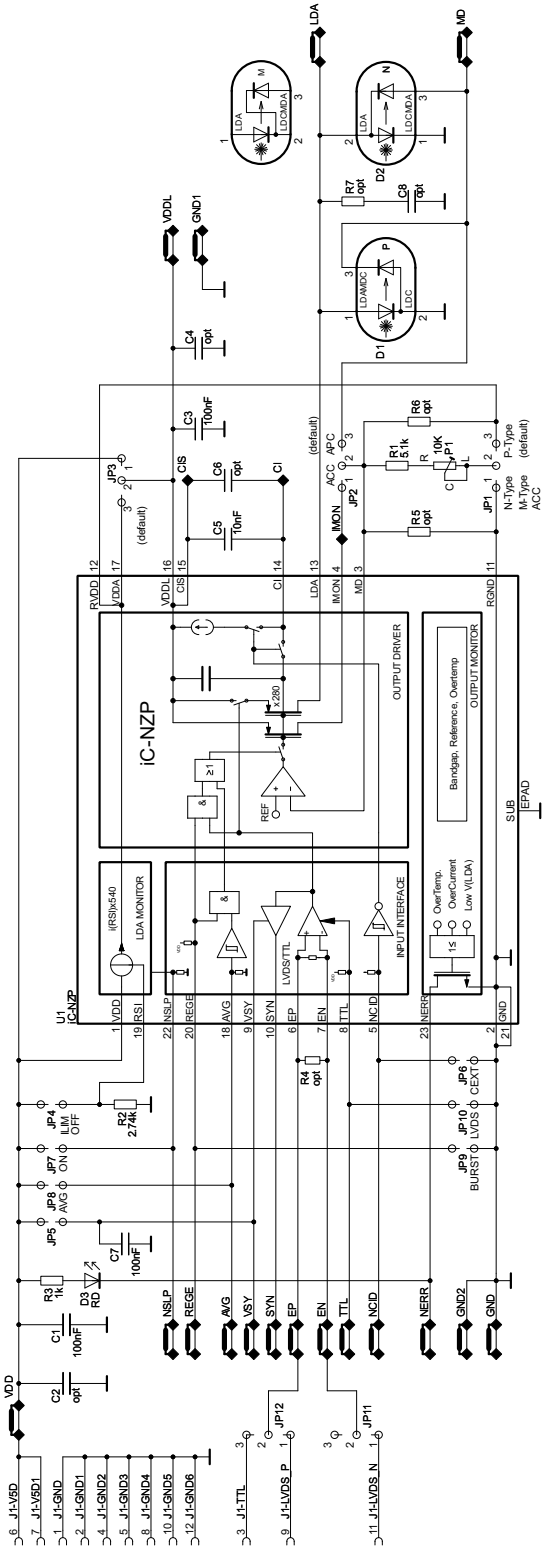


Figure 8: Schematic of the evaluation board

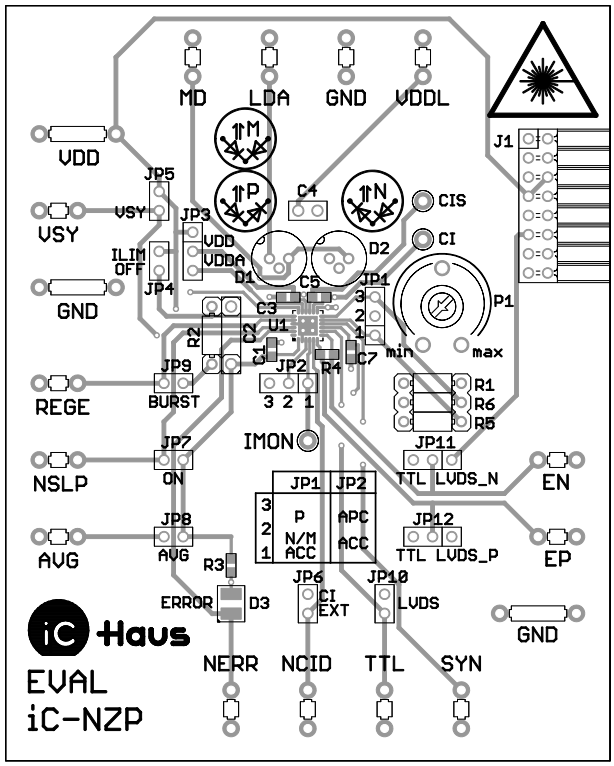


Figure 9: Evaluation board (component side)

ORDERING INFORMATION

Type	Package	Order Designation
iC-NZP	QFN24 4 mm x 4 mm Evaluation Board	iC-NZP QFN24-4x4 iC-NZP EVAL NZP1D

For technical support, information about prices and terms of delivery please contact:

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