iC-MV 8-BIT HALL ENCODER WITH CASCADABLE SERIAL INTERFACE

preliminary

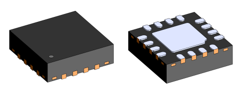
FEATURES

- Integrated Hall sensors with signal conditioning
- Automatic gain control with error detection (loss of magnet)
- 8-bit real-time interpolation for up to 24 000 rpm
- Binary interpolation factors from 2 to 8 bit
- Programmable zero position
- Cascadable serial shift register with SSI compatibility
- Bus-compatible EEPROM I^2C interface
- Space saving features: small 3 mm x 3 mm QFN package, magnet size of Ø 3 mm
- Standby mode
- Extended temperature range of -40...+125 °C

APPLICATIONS

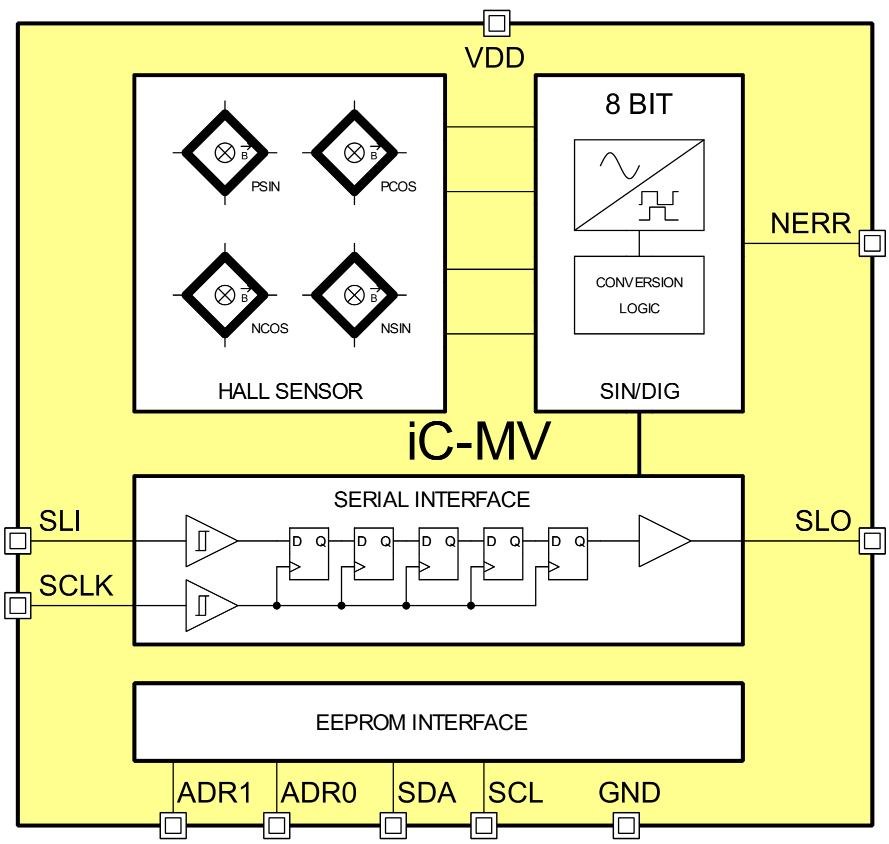
- Absolute multiturn encoders
- Absolute rotary encoders
- Contactless rotary switches

PACKAGES



QFN16
3 mm x 3 mm x 0.9 mm
RoHS compliant

BLOCK DIAGRAM



DESCRIPTION

Magnetic encoder iC-MV has been optimized for multiturn measuring systems with up to four dependent axes and gear reduction ratios of between 1:2 and 1:32.

The sensor generates one sine and one cosine cycle per revolution of the magnet, enabling the angle to be clearly determined by the integrated 8-bit sine-to-digital converter. The internal signal conditioning unit provides a constant signal level that is independent of the magnetic field strength, supply voltage, and temperature. A loss-of-magnet condition can be indicated at alarm output NERR and via the serial interface (SSI protocol with an optional error bit).

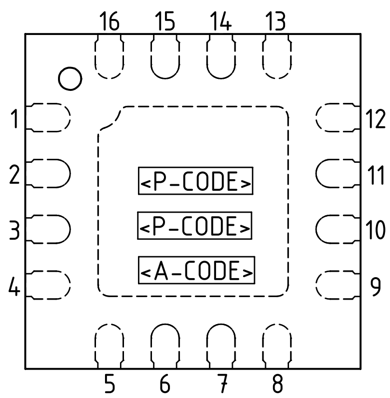
Two to four iC-MVs can be connected in series using their SLI and SLO ports. During data transmission, the position data of the fastest turning iC-MV is sent to the next slowest device. This then corrects its position data to match that of the previous IC and sends this in protocol to the next slowest chip. This procedure provides the SSI master with a multiturn data word that is synchronized with itself. Furthermore, in place of mechanical phase alignment between the gear stages, iC-MV features an offset register to compensate for the phase angle electronically.

All inputs and outputs are protected against destruction by ESD (electrostatic discharge). For test purposes an electric signal coupling is possible at the integrated Hall sensors (e.g. in the ABZ operation).

CONTENTS

PACKAGING INFORMATION

PIN CONFIGURATION QFN16 (3 mm x 3 mm)

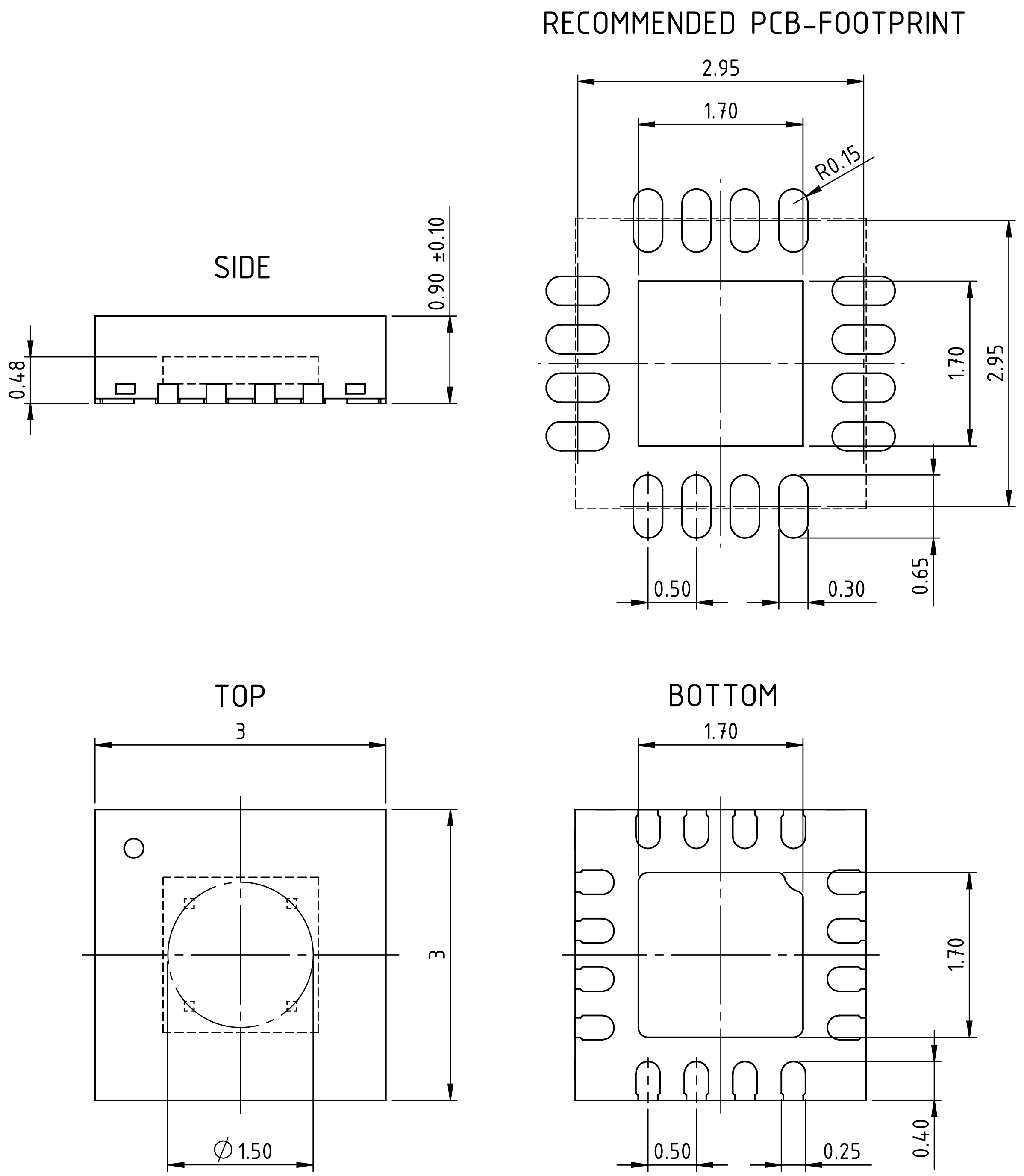


PIN FUNCTIONS

No.	Name	Function
1	n.c.[1]	
2	VDD	+4.5 V to +5.5 V Supply Voltage
3	NERR	Open Drain Error Output (NOSBY = 0x1), Standby Input (NOSBY = 0x0), Analog Output GAIN and NCOS
4	n.c.[1]	
5	ADR1	Address Pin 1 (active hi), Analog Input VTC (MODE)
6	ADR0	Address Pin 0 (active hi), Analog Input VTS (MODE)
7	n.c.[1]	
8	GND	Ground
9	n.c.[1]	
10	SDA	EEPROM Interface, I^2C Data Line
11	SCL	EEPROM Interface, I^2C Clock Line
12	n.c.[1]	
13	SLO	Serial Data Output (SSI), Analog Output PCOS (Analog Out), Threshold Output STOUT, Clock Output CLK (Digital Test), Incremental Output Z (ABZ Operation)
14	n.c.[1]	
15	SLI	Serial Data Input (SSI), Analog Output NSIN (Analog Out) and VREF (Digital Test), Incremental Output A (ABZ Operation)
16	SCLK	Serial Clock Input (SSI), Analog Output PSIN (Analog Out) and Analog Output GAIN (Digital Test), Incremental Output B (ABZ Operation)
	BP	Backside Paddle [2]

IC top marking: <P-CODE> = product code, <A-CODE> = assembly code (subject to changes);
1) Pin numbers marked n.c. are not connected.
2) Connecting the backside paddle is recommended by a single link to GND. A current flow across the paddle is not permissible.

PACKAGE DIMENSIONS



All dimensions given in mm.
Tolerance of sensor pattern: ±0.10mm / ±1° (with respect to center of backside pad).
Tolerances of form and position according to JEDEC MO-220.

drb_qfn16-3x3-1_mv_z1_pack_1, 15:1

ABSOLUTE MAXIMUM RATINGS

These ratings do not imply operating conditions; functional operation is not guaranteed. Beyond these ratings device damage may occur.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	V()	Voltage at VDD		-0.3	6	V
G002	Vpin()	Voltage at ADR1, ADR0, SCL, SDA, SCLK, SLI, SLO		-0.3	6	V
G003	Vscan()	Voltage at NERR for Scan Test Activation		-0.3	8	V
G004	Imx(VDD)	Current in VDD		-10	20	mA
G005	Imx()	Current in NERR, SCL, SDA, SLO		-10	10	mA
G006	Vd()	ESD Susceptibility at all pins	HBM, 100 pF discharged through 1.5 kΩ		2	kV
G007	Tj	Junction Temperature		-40	150	°C
G008	Ts	Chip Storage Temperature		-40	150	°C

THERMAL DATA

Operating conditions: VDD = 4.5...5.5 V

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range		-40		125	°C
T02	Rthja	Thermal Resistance Chip to Ambient	package mounted on PCB, *thermal pad* at approx. 2 cm² cooling area		40		K/W

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating condition: VDD = 5 V ±10 %, Tj = -40...125 °C, 4 mm NdFeB magnet unless otherwise noted.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
General							
001	V(VDD)	Permissible Supply Voltage VDD		4.5		5.5	V
002	I(VDD)	Supply Current in VDD Normal Mode	normal mode (LOPM = 0x0), without load		4	6	mA
003	I(VDD)	Supply Current in VDD Low Power Mode	low power mode (LOPM = 0x1), without load		2	4	mA
004	I(VDD)	Supply Current in VDD	NOSBY = 0x1, NERR = lo		0.6	1.4	mA
005	Vc()hi	Clamp-Voltage hi at SLO, SDA, SCL, ADR0, ADR1, SLI, SCLK	Vc()hi = V() − VPD, I() = 1 mA	0.4		1.5	V
006	Vc()lo	Clamp-Voltage lo at SLO, NERR, SDA, SCL, ADR0, ADR1, SLI, SCLK	I() = -1 mA	-1.5		-0.3	V
Hall Sensor Array and Signal Conditioning							
101	Hext	Permissible Magnetic Field Strength	at chip surface	20		100	kA/m
102	fmag	Operating Magnetic Field Frequency	LOPM = 0x0 LOPM = 0x1			400 50	Hz Hz
103	rpm	Rotating Speed of Magnet	LOPM = 0x0 LOPM = 0x1			24000 3000	rpm rpm
104	dsens	Diameter of Hall Sensor Circle			1.5		mm
105	xdis	Permissible Lateral Displacement of Magnet Axis to Center of Hall Sensors	4 mm magnet			0.2	mm
106	xpac	Displacement Chip Center to Package Center	package QFN16	-0.05		0.05	mm
107	ϕpac	Angular Alignment of Chip vs. Package	package QFN16	-0.6		0.6	deg
108	hpac	Distance Chip Surface to Package Surface	package QFN16		0.4		mm
Automatic Gain Control							
201	tampl	Settling Time of Gain Control	to 70 % of final amplitude		200	500	µs
202	V()gain	Gain Output Voltage	TEST = 0b001 measurable at NERR or TEST = 0b011 measurable at SCLK	0.05		4.0	V
Sine/Digital Converter							
801	RESsdc	Converter Resolution			8		bit
802	AAabs	Absolute Angular Accuracy	Vpp() = 4 V calibrated	-3		3	deg
803	AArel	Relative Angle Error	ideal input signals, quasi static	-15		15	%
Power Down Reset							
901	Vref(SLI)	Reference Voltage	TEST = 0b011	45	50	55	%VDD
902	VDDon	Turn-on Threshold VDD (Power-Up-Enable)	increasing voltage	3.3	3.8	4.4	V
903	VDDoff	Turn-off Threshold VDD (Power-Down-Reset)	decreasing voltage	2.8	3.4	3.8	V
904	VDDhys	Turn-On Threshold Hysteresis		0.3			V
Serial Interface: SCLK, SLO, SLI							
A01	Vs()hi	Saturation Voltage hi	Vs()hi = V(VPD) − V(), I() = -1.6 mA			0.4	V
A02	Vs()lo	Saturation Voltage lo	I() = 1.6 mA			0.4	V
A03	Isc()lo	Short-Circuit Current lo	V() = VDD	10		90	mA
A04	Isc()hi	Short-Circuit Current hi	V() = 0 V	-90		-10	mA
A05	tr()	Rise Time at SLO	CL = 50 pF			60	ns
A06	tf()	Fall Time at SLO	CL = 50 pF			60	ns
A07	Vt()hi	Threshold Voltage hi at SCLK, SLI				2	V

ELECTRICAL CHARACTERISTICS

Operating condition: VDD = 5 V ±10 %, Tj = -40...125 °C, 4 mm NdFeB magnet unless otherwise noted.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
A08	Vt()lo	Threshold Voltage lo at SCLK, SLI		0.8			V
A09	Vt()hys	Threshold Hysteresis at SCLK, SLI		150	250		mV
A10	Ipu()	Pull-up Current at SCLK, SLI	V() = 1 V...VDD	-60	-30	-6	µA
A11	Vpu()	Pull-up Voltage at SCLK, SLI	Vpu() = VDD – V(), I() = -5 µA			0.6	V
A12	fin()	Permissible Clock Frequency at SCLK				2	MHz
A13	t_{tos}	SSI Timeout at SLO		14		29	µs
EEPROM Interface SCL, SDA, ADR0, ADR1							
B01	Vs()lo	Saturation Voltage lo at SCL, SDA	I() = 4 mA			0.4	V
B02	Isc()lo	Short-Circuit Current lo at SCL, SDA		10		90	mA
B03	Vt()hi	Input Threshold Voltage hi				2	V
B04	Vt()lo	Input Threshold Voltage lo		0.8			V
B05	Vt()hys	Input Hysteresis	Vt()hys = Vt()hi – Vt()lo	300	500		mV
B06	Ipu()	Input Pull-up Current at SCL, SDA	V() = 0...VDD – 1 V	-60	-30	-6	µA
B07	Vpu()	Input Pull-up Voltage at SCL, SDA	Vpu() = VDD – V(), I() = -5 µA			0.6	V
B08	fclk()	Clock Frequency at SCL		50	80	100	kHz
B09	tbusy()cfg	Configuration Time	of one iC-MV	1	3	10	ms
B10	Cycle	Number of Stop Sequences at the Beginning of a Communication			8		
B11	Ipd()	Pull-down Current Source at ADR0, ADR1	V() = 1 V...VDD	6	30	60	µA
Oscillator							
C01	fosc()	System Clock	TEST = 0b011, measured at pin SLO	0.8	1.1	1.6	MHz
Error Output / Standby Input NERR							
H01	Vs()lo	Saturation Voltage lo	I() = 4 mA			0.4	mV
H02	Isc()lo	Short-Circuit Current lo	V() = VDD	5		80	mA
H03	Rpu()	Pull-up Resistor	ENPU = 0x1	7	11	15	kΩ
H04	Vt()hi	Input Threshold Voltage hi	NOSBY = 0x1			2	V
H05	Vt()lo	Input Threshold Voltage lo	NOSBY = 0x1	0.8			V
H06	Vt()hys	Threshold Hysteresis	NOSBY = 0x1, Vt()hys = Vt()hi – Vt()lo	150	250		mV
H07	VTMon	Turn-on Threshold Scan Test	increasing voltage at NERR			VDD + 2	V
H08	VTMoff	Turn-off Threshold Scan Test	decreasing voltage at NERR	VDD + 0.5			V
H09	VTMhys	Threshold Hysteresis Scan Test	VTMhys = VTMon – VTMoff		0.03		V

OPERATING REQUIREMENTS: Serial Interface (SSI)

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
SSI						
I001	t_{MAS}	Permissible Clock Period		500	2 x t_{tos}	ns
I002	t_{MASh}	Clock Signal hi Level Duration		250	t_{tos}	ns
I003	t_{MASl}	Clock Signal lo Level Duration		250	t_{tos}	ns

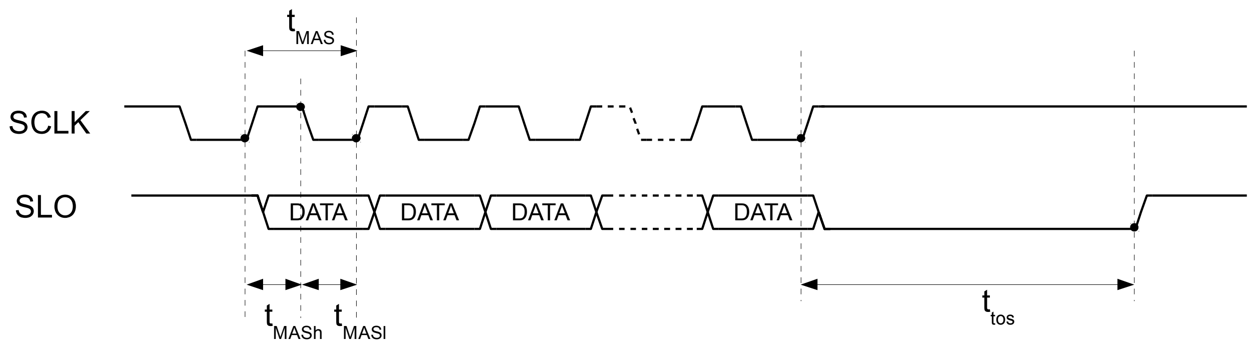


Figure 1: Timing SSI

CONFIGURATION

OFFSET: Offset Position (P. 14)
DIR: Count Direction (P. 14)
RNF: Data Output Edge (P. 14)
EMODE: Errorbit Options (P. 15)
DL: Data Length (P. 15)
ERRSY: Synchronization Monitoring (P. 15)
NOSBY: Standby Enabling (P. 15)
LOPM: Power Saving Operation (P. 15)
ENPU: Pull-up Enabling (P. 15)
SYNC: Position Data Synchronization (P. 15)
MODE: Operating Modes (P. 16)

OVERVIEW								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
iC-MV 1: ADDR = 0b00								
0x00	OFFSET(7:0)							
0x01	DIR	RNF	EMODE(2:0)			DL(2:0)		
0x02	ERRSY	NOSBY	LOPM	ENPU	SYNC	MODE(2:0)		
0x03	-							
iC-MV 2: ADDR = 0b01								
0x04	OFFSET(7:0)							
0x05	DIR	RNF	EMODE(2:0)			DL(2:0)		
0x06	ERRSY	NOSBY	LOPM	ENPU	SYNC	MODE(2:0)		
0x07	-							
iC-MV 3: ADDR = 0b10								
0x08	OFFSET(7:0)							
0x09	DIR	RNF	EMODE(2:0)			DL(2:0)		
0x0A	ERRSY	NOSBY	LOPM	ENPU	SYNC	MODE(2:0)		
0x0B	-							
iC-MV 4: ADDR = 0b11								
0x0C	OFFSET(7:0)							
0x0D	DIR	RNF	EMODE(2:0)			DL(2:0)		
0x0E	ERRSY	NOSBY	LOPM	ENPU	SYNC	MODE(2:0)		
0x0F	CRC(7:0) over Addr = 0x00 bis 0x0E							

Table 5: Register layout

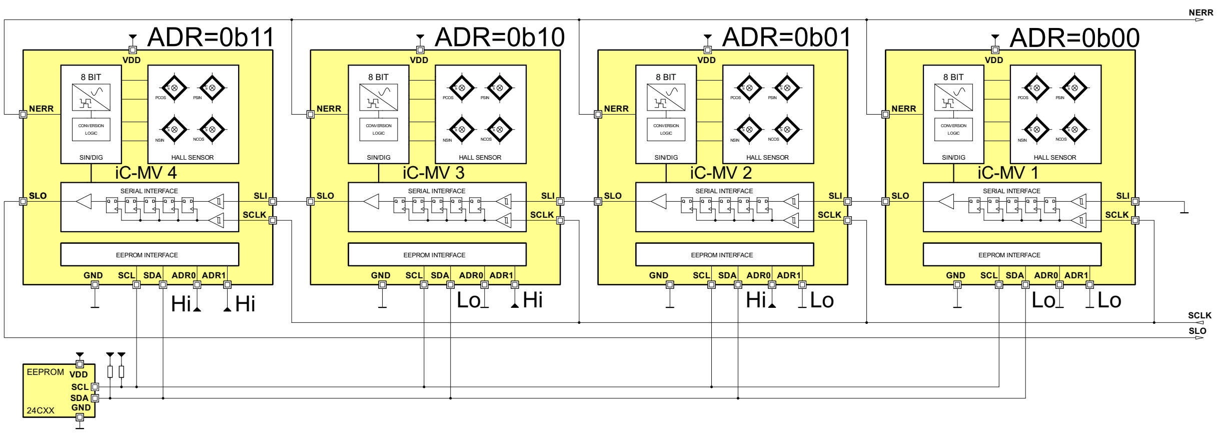


Figure 2: I^{2}C Device Addressing

THE SENSOR PRINCIPLE

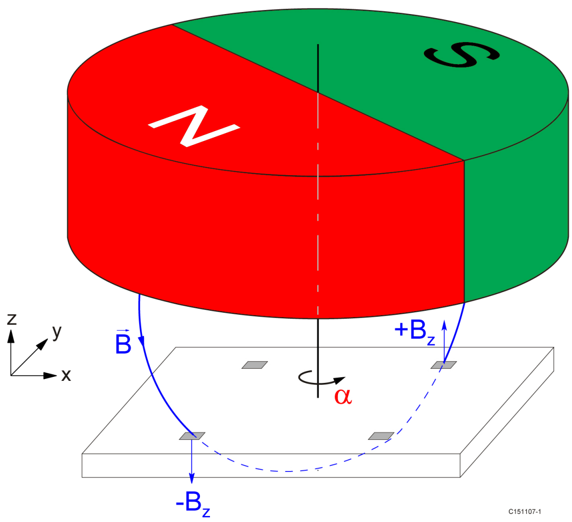


Figure 3: Sensor Principle

Together with a rotating permanent magnet and an EEPROM, iC-MV represents a complete encoder system. Ideal sensor signals are received when using a diametrically magnetized, cylindrical permanent magnet of neodymium iron boron (NdFeB) or samarium cobalt (SmCo). The magnet cylinder's diameter should be within a range of 2 mm to 4 mm.

iC-MV has four Hall sensors adapted for angle determination which convert the magnetic field into measurable Hall voltages. Solely the magnetic field's z component is evaluated at which the field lines pass through two opposing sensors in opposite directions (see Figure 3). The arrangement of the Hall sensors has been specifically selected to allow a very tolerant assembly of iC-MV to the magnet axis.

Differential Hall signals are generated by the combination of two Hall sensors each. When the magnet rotates around its longitudinal axis, sine and cosine voltages are generated which are used for angle determination.

HALL SENSORS AND SIGNAL GENERATION

The four Hall sensors are placed in the center of the QFN16 package in a circle with a diameter of 1.5 mm and have a 90 ° angle distance to one another.

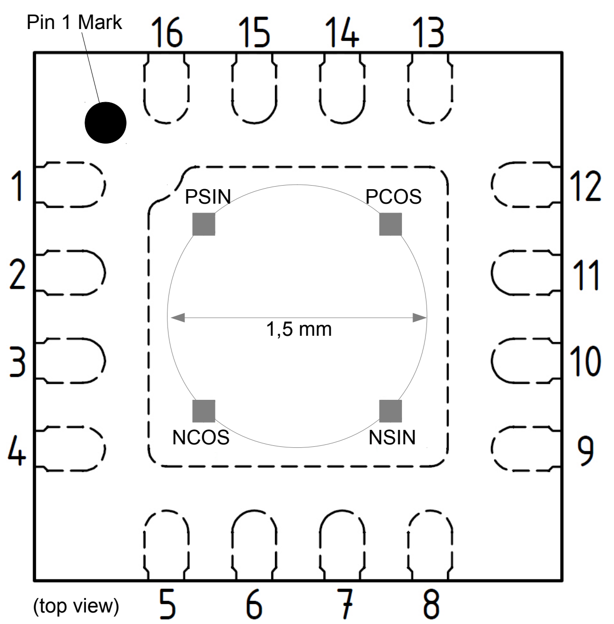


Figure 4: Position of the Hall sensors

When a magnetic south pole approaches the package surface the magnetic field shows a positive component in z direction (i.e. from the top of the package). The individual Hall sensors each generate their own positive signal voltage.

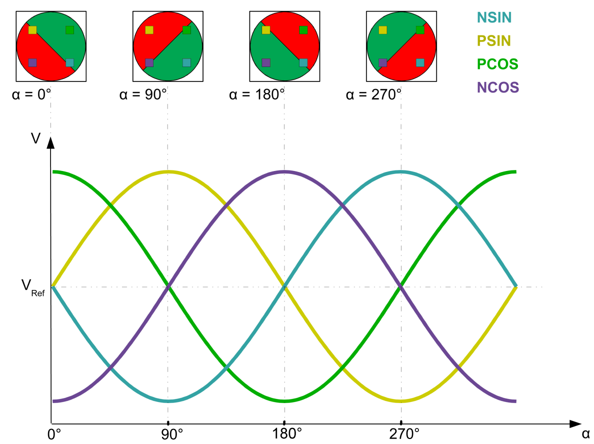


Figure 5: Analog Signals (single ended)

For the determination of the angle position of a diametrically polarized magnet placed above the device, the signal difference of the opposed Hall sensors is generated. This results in the sine being $V_{SIN} = V_{PSIN} - V_{NSIN}$ and the cosine being $V_{COS} = V_{PCOS} - V_{NCOS}$.

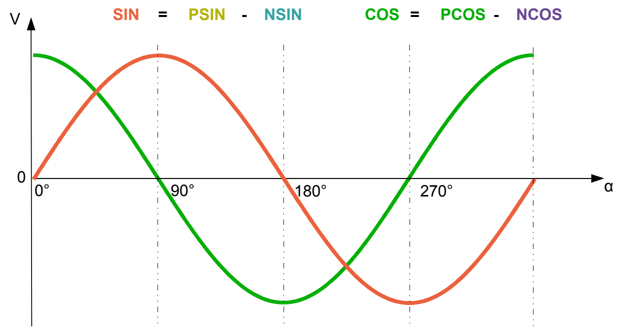


Figure 6: Analog Signals (differential)

The magnet's zero angle position is characterized through the resulting cosine voltage value being maximal and the sine voltage value being zero.

This is the case when the magnet's south pole is located exactly above sensor PCOS and the north pole exactly above sensor NCOS. Sensors PSIN and NSIN are located along the pole threshold so that both do not generate a Hall signal.

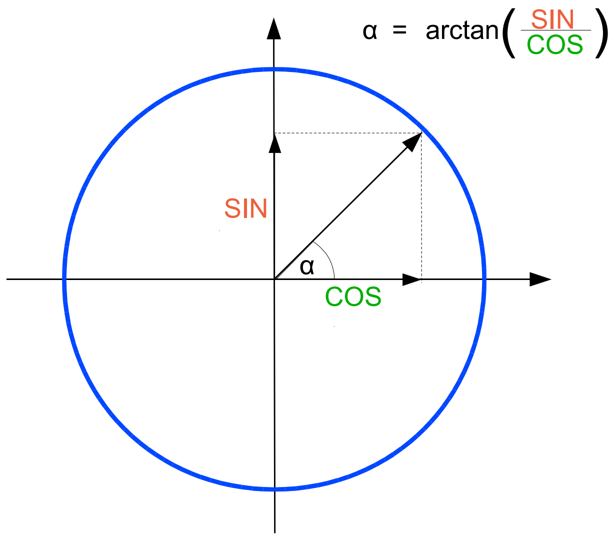


Figure 7: XY Plot and Angle Function

With further clockwise rotation of the magnet the poles then overlap the PSIN and NSIN sensors so that the sine voltage value becomes maximal. Sine and cosine signals are generated which represent the angle position of the magnet α (Figure 7).

All Hall sensor signals can be switched to the outside for test purposes.

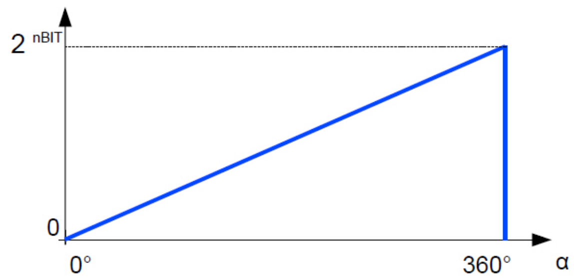


Figure 8: Converter Resolution

MULTITURN PRINCIPLE

iC-MV can form an absolute measuring system over several revolutions, whereby the number of revolutions is saved in the gear. The singleturn's drive shaft activates the first axis in the gear. In the following example the transmission ratio between all axes is: $Ratio = \frac{1}{N}$.

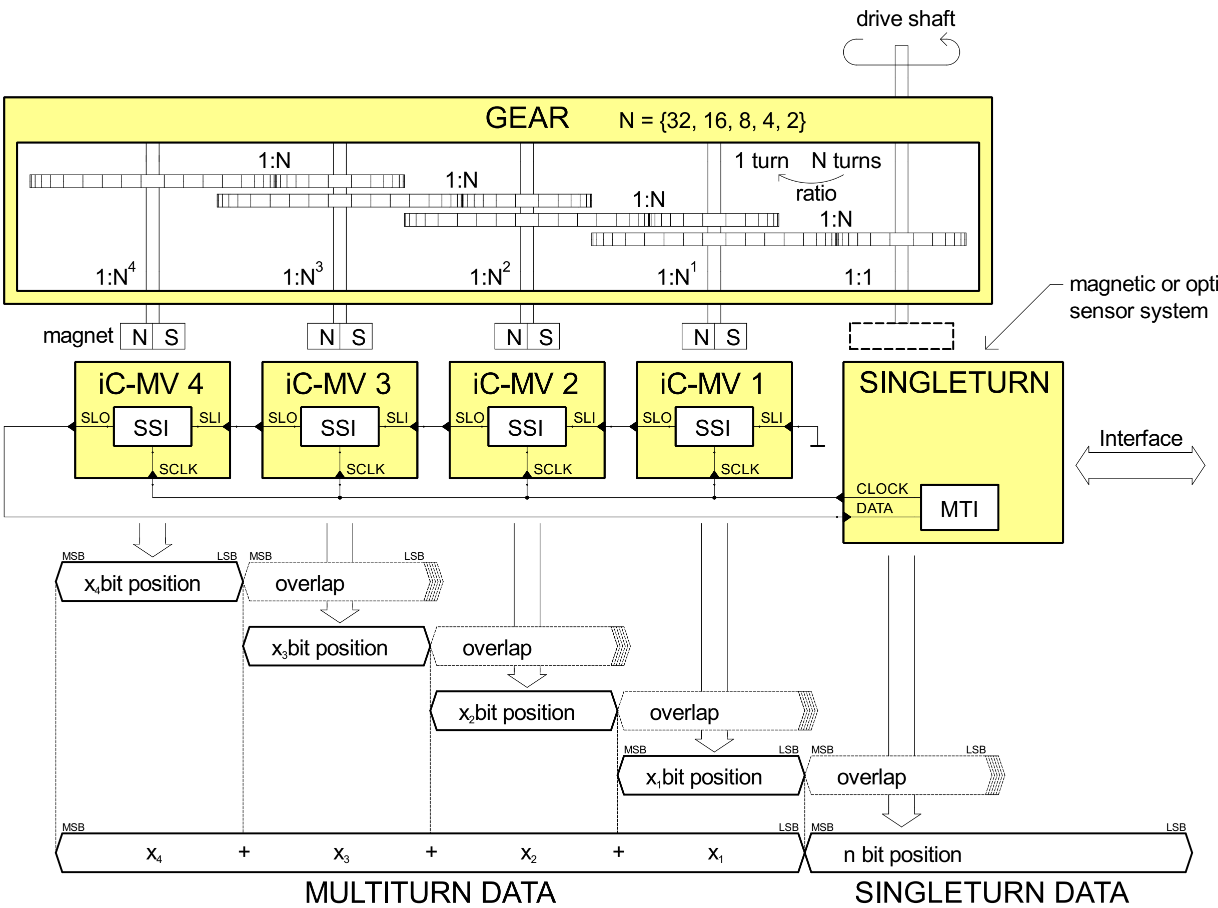


Figure 9: General System and Data Display

The iC-MVs connected in series together constitute a large serial shift register. The entire data length is dependent on the position data length of the individual iC-MVs and on the number of set error bits, as well as on the number of iC-MVs existing in the system. The individual iC-MVs' position data length is dependent on the gear axes' transmission ratio relative to one another. The fourth or last iC-MV in the chain is the first component to transmit its data.

REGISTERS

OFFSET(7:0): Position Offset

The content of the offset register is added to the current position. It allows to adjust the position data in a way that a synchronization of the position data is possible. The functioning and offset calculation is described in the correspondent paragraph.

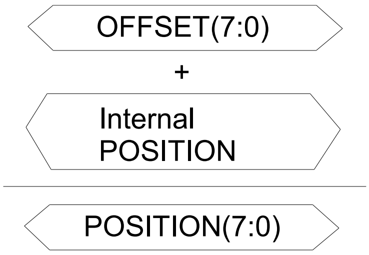


Figure 10: Offset Addition

OFFSET(7:0)	Addr. 0x0; bit 7:0
Code	Description
0x00	0
...	...
0x7F	127
...	...
0xFF	255

Table 6: Position Offset

DIR: Counting Direction

Bit DIR inverts the position register's counting direction and has to be inverted for the counter-rotating axes, so that all iC-MVs then have the same counting direction.

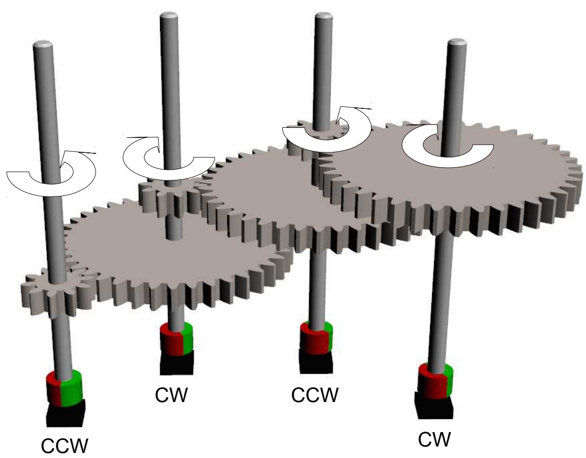


Figure 11: Counting Direction

DIR	Addr. 0x1; bit 7
Code	Description
0x0	Counting direction rising at clockwise rotation (CW)
0x1	Counting direction falling at counterclockwise rotation (CCW)

Table 7: Direction of Rotation

RNF: Edge of Data Output

In the SSI protocol position data is usually output with the rising clock edge at pin SLO. In order to increase the calculation time for components in the chain, position data with the falling clock edge can be output.

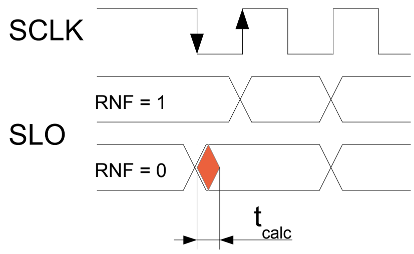


Figure 12: Increasing the Calculation Time

Chain components are to be configured with RNF = 0x0; only the last component (iC-MV 4) is to be configured with RNF = 0x1.

RNF	Addr. 0x1; bit 6
Code	Description
0x0	falling edge
0x1	rising edge

Table 8: Edge of Data Output

EMODE(2:0): Error Bit Options

The EMODE indicates how a faulty condition is displayed. The configuration of the error bit options should be identical with all iC-MVs. As soon as EMODE is configured with 0b001 or 0b011 an error bit is attached to the end of the position data. Each iC-MV manipulates this error bit according to its error status. A faulty status is dominant. With EMODE = 0b111 or 0b101 each iC-MV complements its own error bit at the end of the sensor data.

EMODE(2:0)	Addr. 0x1; bit 5:3
Code	Description
0bXX0	No error bit
0b001	1 serial error bit lo active
0b011	1 serial error bit hi active
0b101	n serial error bit lo active
0b111	n serial error bit hi active

Table 9: Error Bit Options

DL(2:0): Data Length

The data length indicates how many positions of the position register are clocked out. The data length is set independently of the transmission. Thereby, the data length of the first iC-MV in the chain can be selected bigger.

DL(2:0)	Addr. 0x1; bit 2:0
Code	Description
0x00	DL + 1 = 1 bit
...	...
0x02	DL + 1 = 3 bit
0x03	DL + 1 = 4 bit
0x04	DL + 1 = 5 bit
...	...
0x07	DL + 1 = 8 bit

Table 10: Data Length

ERRSY: Synchronization Monitoring

If the synchronization monitoring is activated, an error bit is set as soon as the position data is not consistent. The data length must then be DL = 3.

ERRSY	Addr. 0x2; bit 7
Code	Description
0x0	Synchronization monitoring deactivated
0x1	Synchronization monitoring activated

Table 11: Synchronization Monitoring

NOSBY: Standby Enable

If the NOSBY bit is not set, iC-MV can be switched to standby operation via pin NERR. The position data is thereby maintained. In case of a faulty configuration, iC-MV remains in standby enable.

NOSBY	Addr. 0x2; bit 6
Code	Pin function NERR
0x0	Standby input (hi active)
0x1	Error output (lo active)
Note	Consider configuration of ENPU.

Table 12: Standby Enable

LOPM: Low Power Mode

The low power mode minimizes the sampling rate and thereby reduces the current consumption of iC-MV to approx. 2 mA.

LOPM	Addr. 0x2; bit 5
Code	Description
0x0	Low power mode deactivated
0x1	Low power mode activated

Table 13: Low Power Mode

ENPU: Pull-up Enable

Bit ENPU activates the pull-up resistor of approx. 11 kΩ at pin NERR.

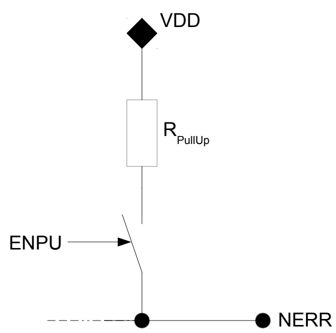


Figure 13: Pull-up Resistor

ENPU	Addr. 0x2; bit 4
Code	Description
0x0	Pull-up deactivated
0x1	Pull-up activated
Note	Consider configuration of NOSBY.

Table 14: Pull-up Enable

SYNC: Position Data Synchronization

The SYNC bit activates the synchronization of the position data. If the SYNC bit is deactivated, the position data is output unaltered.

SYNC	Addr. 0x2; bit 3
Code	Description
0x0	Synchronization deactivated
0x1	Synchronization activated
Note	SYNC = 0x1 shifts the zero pulse in ABZ operation to a length of 180 °.

Table 15: Position Data Synchronization

Note:
A calculated offset correction is required for successful synchronization.

MODE(2:0): Operating Mode
For the testing of individual functions several operating modes are integrated, which are selected via the MODE register.

Output signals according to operating mode									
Operating Mode	MODE(2:0)	**Pin ADR0**	**Pin ADR1**	**Pin SLI**	**Pin SCLK**	**Pin SLO**	**Pin SDA**	**Pin SCL**	**Pin NERR**
Normal Operation	0x00	ADR0	ADR1	SLI	SCLK	SLO	SDA	SCL	NERR
Adjustment	0x01	ADR0	ADR1	SLI	SCLK	SLO	SDA	SCL	GAIN
Analog Out	0x02	VTS	VTC	NSIN	PSIN	PCOS	SDA	SCL	NCOS
Digital Test	0x03	VTS	VTC	VREF	GAIN	CLK	0	0	NERR
Function Test	0x04	VTS	VTC	SLI	SCLK	SLO	SDA	SCL	NERR
Threshold Test	0x05	ADR0	ADR1	SLI	SCLK	STOUT	SDA	SCL	NERR
Converter Test	0x06	VTS	VTC	A	B	Z	SDA	SCL	NERR
ABZ Operation	0x07	ADR0	ADR1	A	B	Z	SDA	SCL	NERR

Table 16: Operating Modes

- **Normal Operation**
  At programming of MODE = 0x00 iC-MV is in normal operation. iC-MV is addressed via ADR(1:0). The position data can be read via pin SLO and pin NERR is configured as standby enable. The signal feed occurs magnetic.

- **Adjustment**
  MODE = 0x01 serves as adjustment. Thereby the automatic gain control's signal gain is output as voltage at pin NERR. This process serves as distance control. The pull-up resistor should be switched off via the ENPU bit.

- **Analog Out**
  With MODE = 0x02 sine and cosine voltage signals can be introduced to the Hall sensors via pins ADR1 and ADR0. The required offset signal is first measured at ADR1 and ADR0. In Analog Out operation the sine/cosine signals are made available in front of the interpolator at pins SLI, SCLK, SLO and NERR.

- **Digital Test**
  For testing the saturation voltage pins SDA and SCL are set to 'lo' in MODE = 0x03. The oscillator clock, V(Vref) and the gain signal are made available. CLK, gain and VREF can be measured in the digital test. The gain signal can be monitored when applying the VTS and VTC voltages.

- **Function Test**
  In MODE = 0x04 signals are fed in via ADR1 and ADR0 just like in MODE = 0x02. The function test has the same function as the normal operation, however, the signal feed occurs electrically. In this test operation e.g. the interpolator can be tested.

- **Threshold Test**
  MODE = 0x05 serves for testing the input circuit threshold. NOSBY bit has to be programmed to 0x0 so that the NERR pin is configured as input. In this operating mode the threshold of the pins is tested. The input pins' thresholds can be determined at STOUT.

- **Converter Test**
  With MODE = 0x06 the converter test is activated. Sine and cosine voltage signals are introduced via ADR1 and ADR0 and the incremental signals are output at SLI, SCLK and SLO.

- **ABZ Operation**
  MODE = 0x07 has the same function as the normal operation. The position output occurs incrementally at pins SLI, SCLK and SLO. NOSBY bit has to be programmed to 0x1 so that the NERR pin is configured as output.

EEPROM INTERFACE and DEVICE ADDRESSING

An external EEPROM is required for the configuration of iC-MV. In the typical multiturn application up to four iC-MVs share one EEPROM. iC-MV 1 is assigned a low level at pins ADR1 and ADR0. Thus, 00b0 is the address of the first iC-MV in the SSI chain. iC-MV 2 is assigned a low level at ADR1 and a high level at ADR0 and hence the address 0b01 (see Figure 2). The addresses for following iC-MVs can be generated from Table 18 according to this principle.

Depending on the address each iC-MV has a different address range for its configuration. At address 0xF the CRC checksum (polynomial 0x11D / start value = 1) is valid for the entire 15 byte. Each iC-MV checks this CRC byte. In case of an error the reading process is restarted. Pin SLO provide to SSI interface and pin NERR provide high level until a successful startup (CRC check OK) is reached. The data at address 0x03, 0x07 and 0x0B is not used.

At the beginning of every communication eight bus cleaning cycles are run through, i.e. stop sequences are being sent in order to reset a possibly remaining slave.

Pin ADR1	Pin ADR0	EEPROM Address Range
lo	lo	iC-MV 1: 0x00 - 0x03
lo	hi	iC-MV 2: 0x04 - 0x07
hi	lo	iC-MV 3: 0x08 - 0x0B
hi	hi	iC-MV 4: 0x0C - 0x0F

Table 17: Address Range

<table>
<tr><th colspan="5">Devices and Addressing</th></tr>
<tr><td>Number of iC-MV</td><td>1</td><td>2</td><td>3</td><td>4</td></tr>
<tr><td>iC-MV 1</td><td>0b00</td><td></td><td></td><td></td></tr>
<tr><td>iC-MV 2</td><td colspan="2">0b01</td><td></td><td></td></tr>
<tr><td>iC-MV 3</td><td colspan="3">0b10</td><td></td></tr>
<tr><td>iC-MV 4</td><td colspan="4">0b11</td></tr>
</table>

Table 18: Address Allocation

SERIAL INTERFACE (SSI)

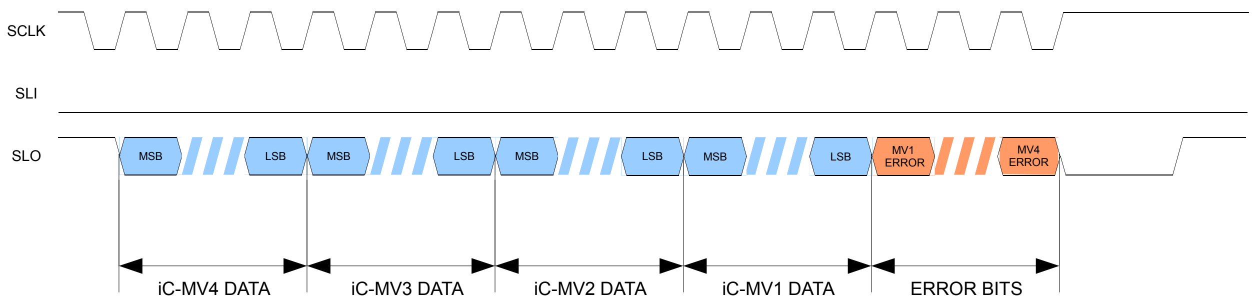


Figure 14: SSI protocol

Two to four iC-MV devices are serially cascaded with their SLI and SLO ports and are each connected with clock SCLK. During an SSI transmission iC-MV 1's position data is transferred to iC-MV 2 and so on up until the master. This principle is illustrated in Figure 9. Each iC-MV synchronizes its position data to the predecessor and sends them to the next device. The SSI master thus receives internally synchronized multiturn data. The number of data bits to be transmitted is determined by the data length DL(2:0). During synchronization the MSB of the preceding iC-MV is compared to the own synchronization bit and the position value is corrected by one, if necessary. This requires the iC-MV's offset register to be programmed correctly.

ABZ INTERFACE

In MODE = 0x07 the ABZ interface is activated. An incremental output occurs at SLI, SCLK and SLO. In ABZ mode register bit SYNC extends the zero pulse about 90°. The resolution can be adjusted via DL(2:0) like in normal operation. The converter hysteresis is 1.4° and the minimum threshold distance is two oscillator clocks.

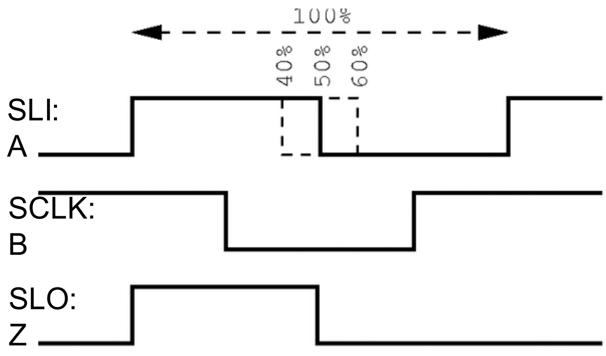


Figure 15: ABZ Signals

ADJUSTMENT

For the adjustment test mode is activated via MODE = 0x01. The automatic gain control's signal gain is output at pin NERR. In this test mode ENPU = 0x0 and NOSBY = 0x1 must be set. The signal level on the signal gain serves as measurement for the axial adjustment between iC-MV and the magnet.

Adjustment: Axial
The GAIN signal should be set between 100 mV and 200 mV via axial adjustment. This equals a distance of about 1 mm.

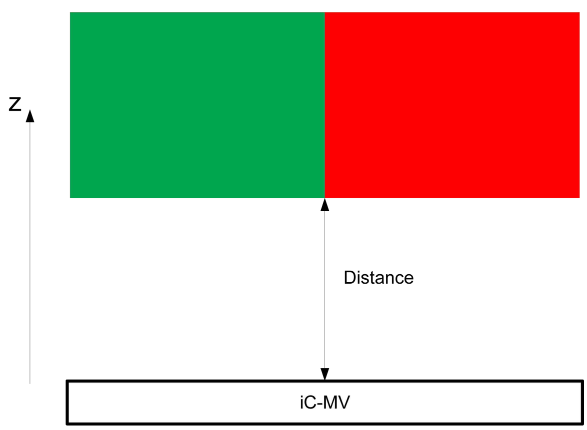


Figure 16: Axial Adjustment

Justage: Radial
The radial adjustment is determined by the mechanical arrangement of the system components (package, gear, axis offset and PCB).

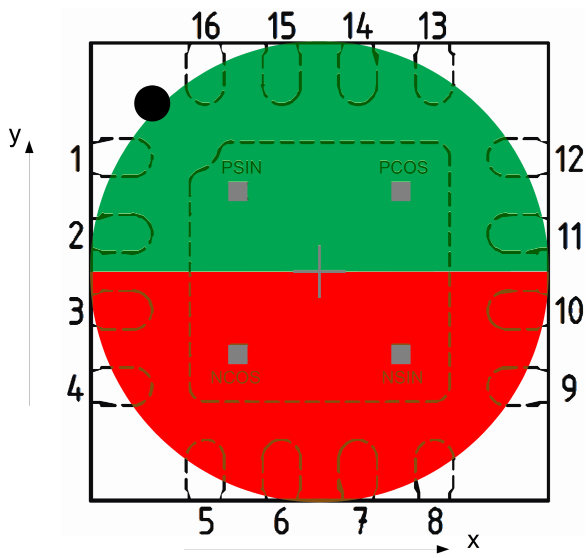


Figure 17: Radial Adjustment

SYNCHRONIZATION

Step 1: Set configuration offset calculation
SYNC = 0x0
OFFSET = 0x00
DL = 0x07 (8 bit data length)

Step 2: Read position data and calculate offset

Offset calculation for ratio = 1:16						
OFFSET		HIDATA (4 bit)		LODATA (4 bit)		90 ° reserve
OFFSET 1	=	singleturn HIDATA	-	iC-MV 1 LODATA	+	4
OFFSET 2	=	iC-MV 1 HIDATA	-	iC-MV 2 LODATA	+	4
OFFSET 3	=	iC-MV 2 HIDATA	-	iC-MV 3 LODATA	+	4
OFFSET 4	=	iC-MV 3 HIDATA	-	iC-MV 4 LODATA	+	4

Table 19: Offset Calculation for Ratio = 1:16

Step 3: Set configuration for ratio = 1:16
SYNC = 0x1
OFFSET = Calculation with offset positions from Table 6
DL = 0x03 (4 bit data length)

Synchronization Monitoring
If bit ERRSY is activated the synchronized position data is checked for consistency. The error is displayed via the error bit in the SSI protocol, if configured. Synchronization monitoring only works with DL = 0x03.

ERROR HANDLING

CRC Error

If the EEPROM is not read out at all or not entirely or if a CRC error is detected, the SSI interface provides a steady high level at request.

EMODE	Addr. 0b01; bit 5:3
Code	Function
0bXX0	No error bit
0b001	1 serial error bit lo active
0b011	1 serial error bit hi active
0b101	n serial error bits lo active
0b111	n serial error bits hi active

Table 20: Error Bit Options

Error Bit Options

If an amplitude error is recognized e.g. through the loss of the magnet, this is displayed through a low level and sent to the SSI protocol, if activated. The error bit is configured via register bits EMODE(2:0), where *n* is the number of the iC-MV slaves.

The error bit is added to the position data. Thereby iC-M 1 in the SSI chain sends its error bit first. In case additional iC-MVs exist, iC-MV 2 then sends its error bit to the neighboring component.

SCAN TEST

In order to test digital components a scan path is integrated. The scan test is activated when a voltage of approx. 1 V above VDD is connected to pin NERR.

SCAN TEST	
Pin	Description
SCLK	Scan Clock
SLI	Scan Input
SLO	Scan Output
ADR1	Scan Enable
ADR0	Not Reset

Table 21: Pin Function in the Scan Test.

APPLICATION EXAMPLES

iC-MHM with 4 iC-MVs

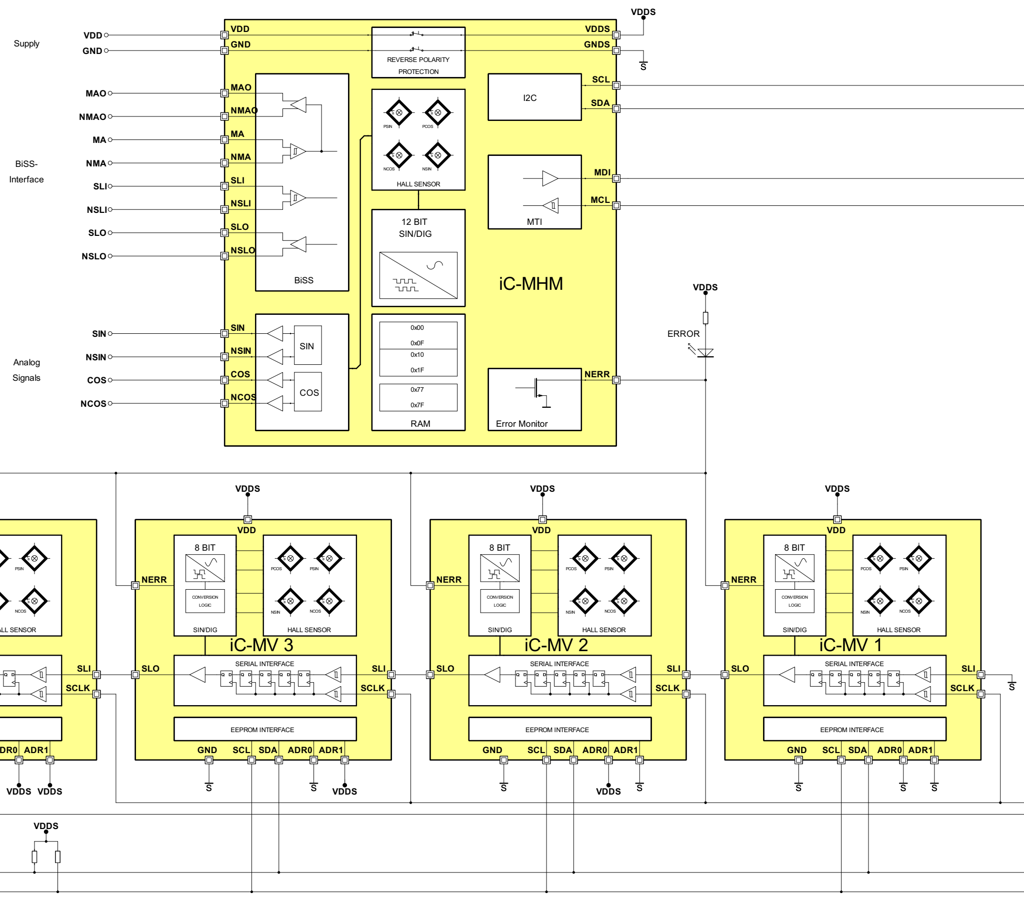


Figure 18: iC-MHM with 4 iC-MVs

iC-MN with 3 iC-MVs

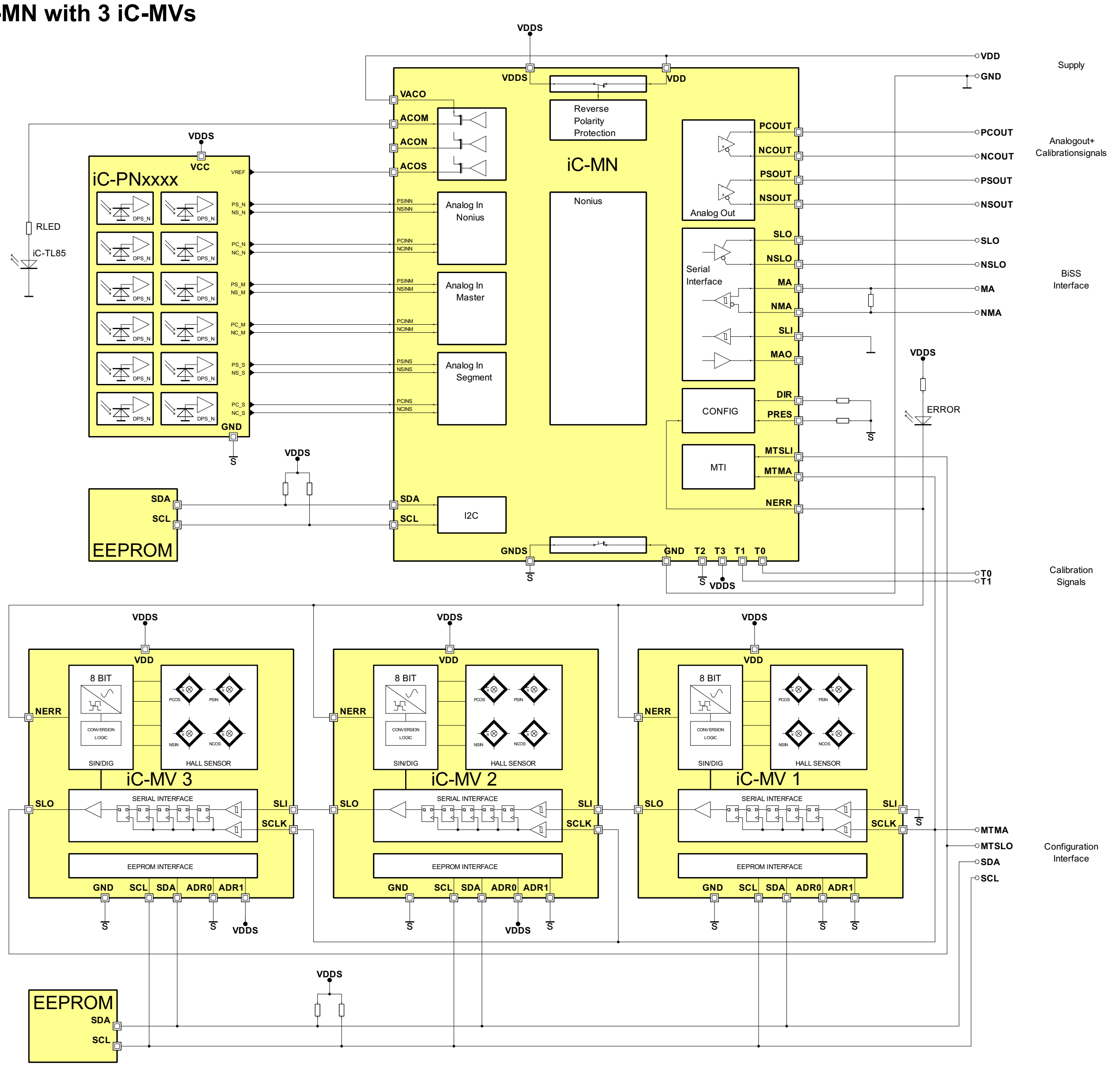


Figure 19: iC-MN with 3 iC-MVs

iC-MU with 3 iC-MVs

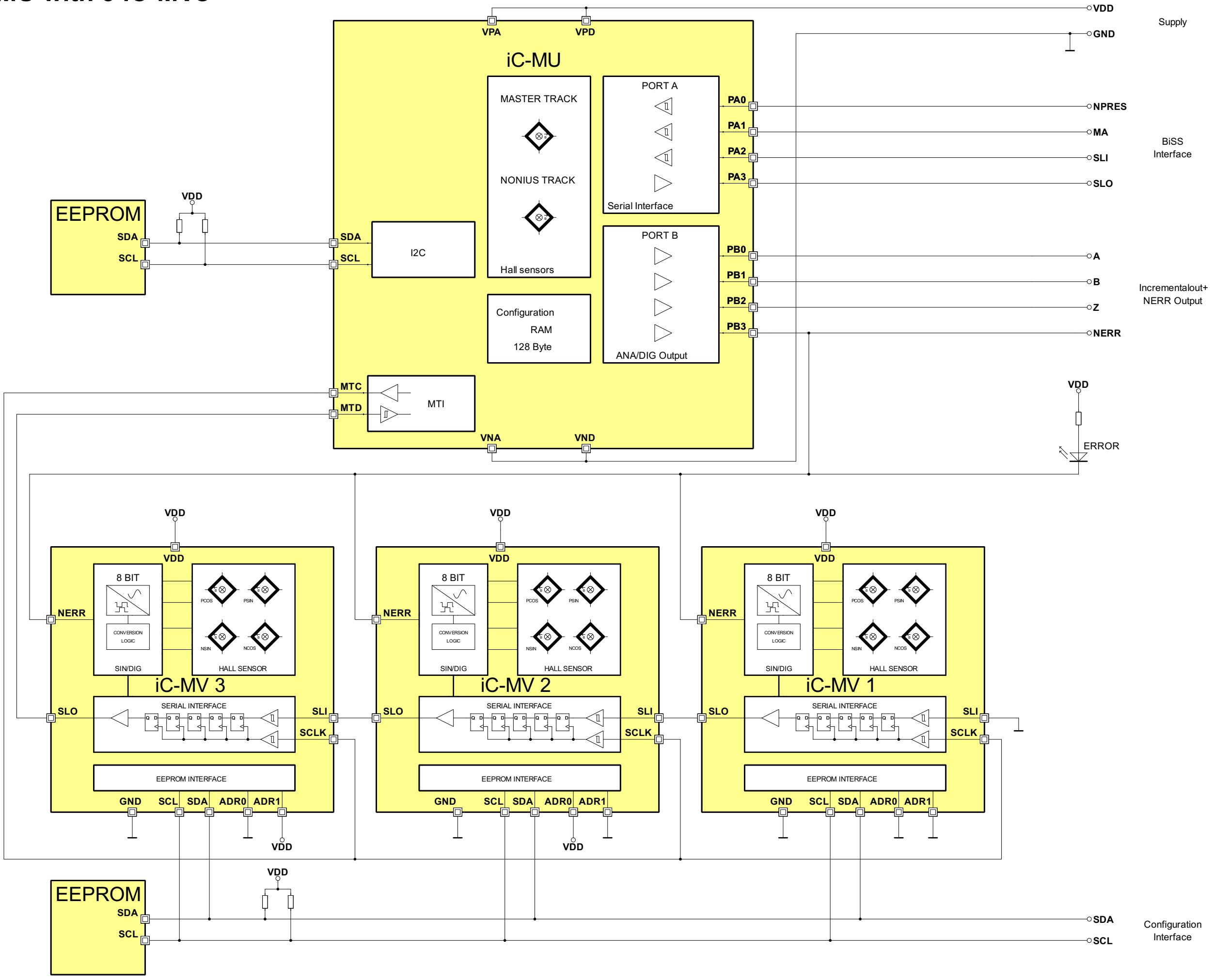


Figure 20: iC-MU with 3 iC-MVs

iC-LGC with 3 iC-MVs

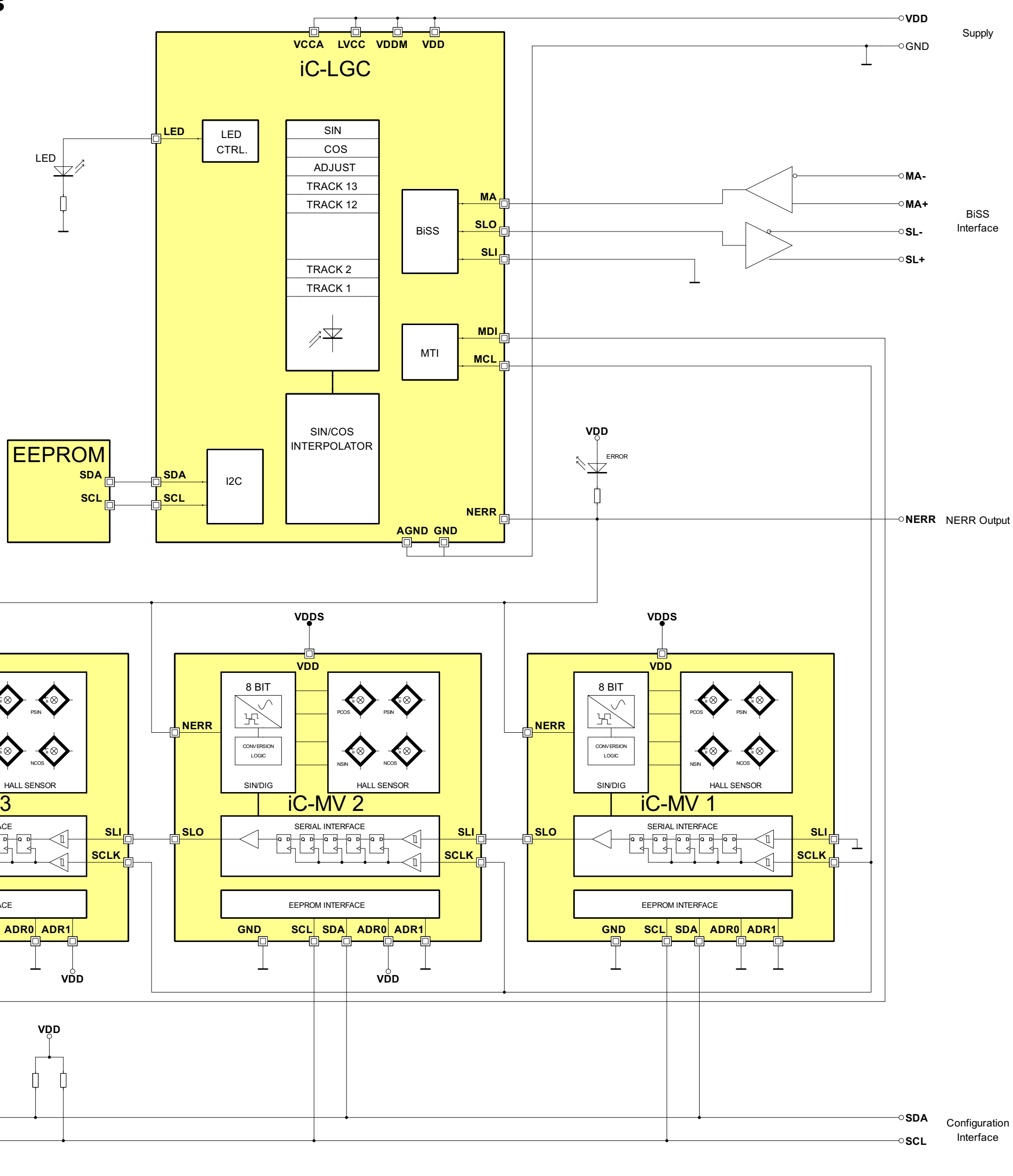


Figure 21: iC-LGC with 3 iC-MVs

MV1A with 4 iC-MVs

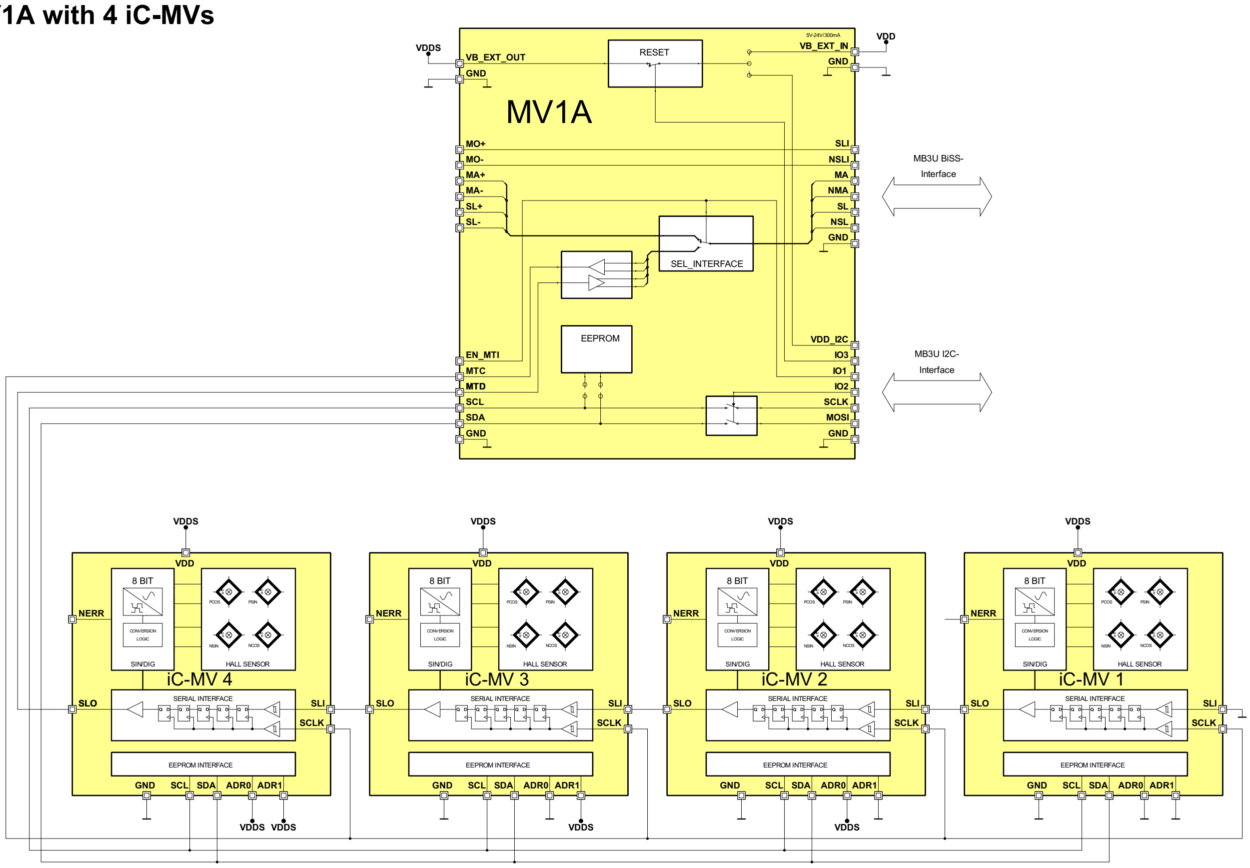


Figure 22: MV1A with 4 iC-MVs

REVISION HISTORY

Rel	Rel.Date	Chapter	Modification	Page
A1	14-08-05	All	Initial release	All

Rel	Rel.Date	Chapter	Modification	Page
A2	15-03-02		Title revised	

ORDERING INFORMATION

Type	Package	Order Designation
iC-MV	QFN16, 3 mm x 3 mm x 0.9 mm RoHS compliant	iC-MV QFN16-3x3

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